Design of Electronic Control Circuit of Piezo-Electric Resonators for sigma delta Modulator Loop in AMS Bi-CMOS 0.35μm

Mohammad Javidan, Philippe Benabes

Design of Electronic Control Circuit of Piezo-Electric Resonators for $\Sigma\Delta$ Modulator Loop in AMS Bi-CMOS 0.35μm

Mohammad Javidan
Department of Signal Processing and Electronics
SUPELEC
91190 Gif/Yvette, FRANCE
Email: mohammad.javidan@supelec.fr

Philippe Benabes, $Member$, $IEEE$
Department of Signal Processing and Electronics
SUPELEC
91190 Gif/Yvette, FRANCE
Email: philippe.Benabes@supelec.fr

***Abstract*— Most of the recent design methodologies of continuous-time sigma-delta modulators use piezo-electric resonators as loop filters. Compared with classical resonators (Gm-c, Gm-LC and etc), piezo-electric resonators have the advantage of high quality factor and accurate resonance frequency. However, they suffer from anti-resonance frequency and impedance adaptation issues with connected electronic circuits. Therefore, their performance is in practice deteriorated. Compatible electronic control circuit is required to achieve expected performance. In this study, the specifications of the electronic control circuit are studied and this circuit is designed in AMS Bi-CMOS 0.35μm technology. the simulations are done at layout-level.**

I. Introduction

The increasing demand for large-band high-speed high-resolution Analog-to-Digital Converters (ADCs) has fed the development of Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulators [1]. Although CT modulators are good candidates when low-power, high-speed and small-size are of critical importance [2], they are highly sensitive to the performance of analog components [3]. One of the most important components is the resonator. A resonator is generally characterized by its Quality factor (Q-factor) and its resonance frequency (f_r).

The influence of the resonator parameters on the modulator performance can be studied through the in-band quantization noise power (P_{NTF}) of the modulator [1]. In the case of a 6^{th}-order classical wide-band $\Sigma\Delta$ modulator with an Over-Sampling-Ratio (OSR) equal to 64, the variation of P_{NTF} versus Q-factor is shown in Fig.1. Noted that, a 6^{th}-order modulator contains three resonators. A large Q-factor is required to ensure the resolution while wide-band electronic constraints allows a maximum of Q-factor up to tens. Now assuming that the Q-factor is an infinite number. Also the distance between the side resonators resonance frequency (f_{r1} and f_{r3}) and the central one (f_{r2}) is symmetric. Mismatch factor of the resonator resonance frequency (λ) can be defined as follows:

$$\lambda = \frac{|f_{r1} - f_{r2}|}{\Delta f} = \frac{|f_{r2} - f_{r3}|}{\Delta f}, \qquad (1)$$

where Δf is equal to $\frac{f_s}{\text{OSR}}$ and f_s is the modulator sampling frequency. In [4], it is demonstrated that for 6^{th}-order $\Sigma\Delta$ modulators the optimal λ is equal to $\sqrt{\frac{3}{5}}$. Fig.2 shows the variation of P_{NTF} of a 6^{th}-order classical wide-band $\Sigma\Delta$ modulator with an OSR equal to 64 versus λ.

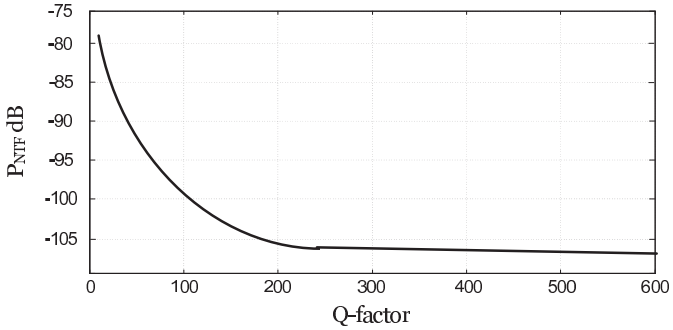

Fig. 1. The variation of P_{NTF} of a 6^{th}-order classical wide-band MSCL $\Sigma\Delta$ modulator versus the resonator Q-factor for an OSR=64.

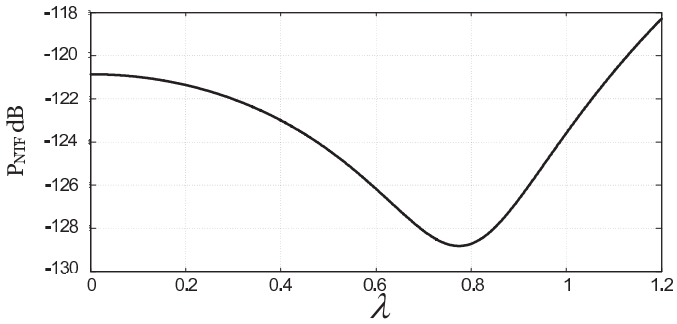

Fig. 2. The variation of P_{NTF} of a 6^{th}-order classical wide-band MSCL $\Sigma\Delta$ modulator versus λ for $Q = \infty$ and OSR=64.

As it is shown, the performance of a 6^{th}-order modulator is highly sensitive to the variation of the resonator characteristics. This variation is inevitable since analog components are sensitive to process parameters, temperature variation, impedance mismatch and etc. However, the variation of the resonator parameters can be decreased by choosing a resonator structure able to perform an accurate resonance frequency with no need of tuning associated with a robust electronic control device

protecting the resonator performance.

The outline of this paper is as follows. In section II the advantages of piezo-electric resonators compared with other types of resonators is explained. In section III a robust electronic control compatible with piezo-electric resonators is proposed. In section IV the results of the design at layout-level in AMS Bi-CMOS 0.35μm technology are presented. Finally, conclusions are presented in section V.

II. Characteristics of Piezo-Electric Resonators

As it is shown in Fig. 1, a Q-factor around 100 is a good compromise between the resolution and practical issues. However, it is out of reach by classical resonators (Gm-C, Gm-LC, AOP-C and etc) even if Q-enhancement circuits are used [5]. Power consumption, non-linearity due to the Q-enhancement circuits and the sensitivity of the resonance frequency to the manufacturing process and temperature variations are the other disadvantages of these kinds of resonators. Therefore, $\Sigma\Delta$ modulators based on classical resonators are not capable of satisfactory performance [6].

Accurate resonators with high Q-factor can be implemented by piezo-electric resonators like Surface Acoustic Wave (SAW) [2] resonators, Bulk Acoustic Wave (BAW) resonators [7] and Lamb Wave Resonators (LWR) [8]. In general, the model of Fig.3 is used to model a piezo-electric resonator around its fundamental resonance frequency. R_m, C_m and L_m are the motional resistance, capacitance and inductance, respectively. C_0 is the inherent static capacitance between the input and the output electrodes.

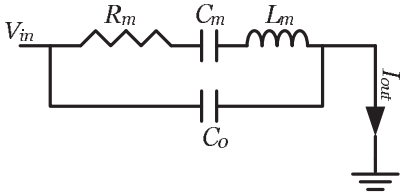

Fig. 3. The equivalent model of a one-port piezo-electric resonator.

Due to the parasitic capacitance (C_0), piezo-electric resonators do not have an ideal second-order resonator transfer function. Fig. 4 shows the frequency response of a typical LWR (table I). Moreover, piezo-electric resonators are passive devices driven in voltage-mode and the resonator gain must be provided through the control circuit. Also, impedance adaptation for the input and the output connections is necessary to maintain the resonator Q-factor and resonance frequency. On the other side, $\Sigma\Delta$ modulator contains several nodes where the output of different components must be added together. Hence, modulator works in current mode because the add function can be done easily by mixing the signal paths with no need of extra enhancement. This means that the resonator control circuit input has to be in current-mode.

The issues can be overcome by using the topology of Fig.5.a [5] where x denotes the resonator. Two symmetrical capacitive paths (C_c) are added and driven in differential-mode. C_c acts, effectively, as a negative capacitance. If C_c is equal to C_0, the anti-resonance frequency is removed. The influence of mismatch between C_0 and C_c is studied in [5]. The first buffer is a trans-impedance circuit converting the input current to the driving voltage and provides the resonator gain and the input impedance adaptation. The second buffer is a current-to-current converter providing the output impedance adaptation. Although the first buffer output impedance (Z_{b1}) and the second buffer input impedance (Z_{b2}) are practically never equal to zero, they must be sufficiently small compared with the resonator impedance at f_r. Small Z_{b1} and Z_{b2} results in a small impedance of the cancellation path ($Z_{b1} + \frac{1}{C_c s} + Z_{b2}$). This is disturbing when the input signal contains high frequency components (like pulse wave signals) because the cancellation path demands a strong current and the buffer must be able to provide correctly this current. This is the case, especially, for the first resonator of the $\Sigma\Delta$ modulator where one of the inputs is the output of a digital-to-analog converter [5]. Fig. 6 shows the driving voltage and the required current of the first resonator of a 6^{th}-order modulator simulated in transistor-level in [5]. Noticeably, a compatible control circuit is required to drive the required current.

TABLE I

LWR typical characteristics [5]

f_r	R_m	C_m	L_m	C_0
100 MHz	100 Ω	212 fF	12 nH	1.8 pF

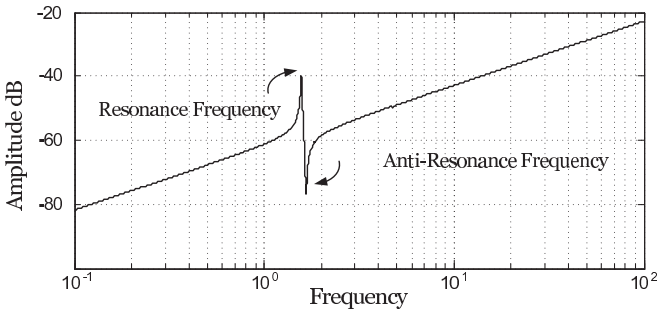

Fig. 4. The frequency response of a typical LWR (table I).

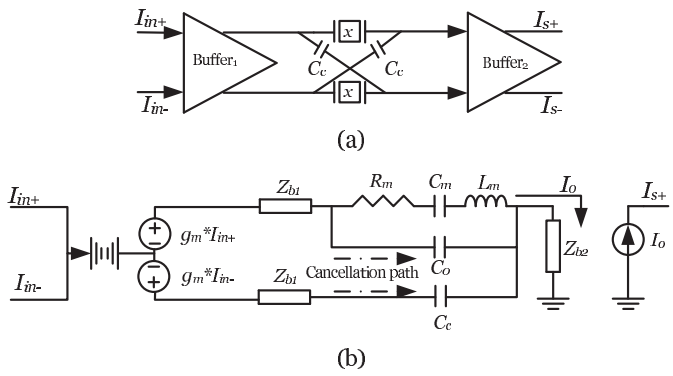

Fig. 5. The proposed electronic control topology (a) and the equivalent model of the positive path (b).

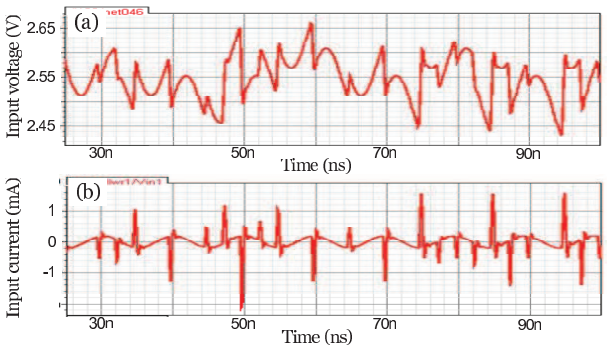

Fig. 6. The driving voltage (a) and the required current (b) of the first resonator of a 6^{th}-order modulator simulated in transistor-level in [5].

III. Transistor-Level Implementation

The design of the resonator electronic control circuit is done in the context of a 6^{th}-order single-stage feed-forward band-pass CT $\Sigma\Delta$ modulator working at $f_c = 0.25 f_s$ (f_c being the modulator central frequency) where f_s is equal to 400 MHz [5]. The current and voltage full-scales are, respectively, equal to $\pm 100\ \mu A$ and $\pm 0.25\ v$. The parameters of the used LWR are given in table I.

The schematic of the positive path of buffer$_1$ is shown in Fig.7. The input current is converted to voltage through R_1. C_1 is used to smooth the output signal and reduce the overshoot in high frequencies. D_1 and D_2 are used to make V_{in} as constant as possible since the linearity depends on the V_{in} constancy. A common-collector arrange (T_2), offering low output impedance, is used as the output stage. Through the π-hybrid model of BJTs, the output impedance is equal to $\frac{1}{g_m} + r_e$ and it can be reduced by increasing the current.

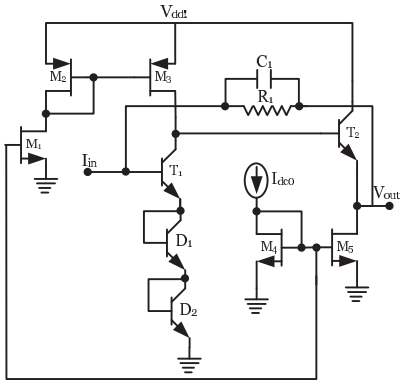

Fig. 7. The proposed schematic for buffer$_1$.

The performance of buffer$_1$ loaded by LWR is shown in Fig. 8. Although a non-zero output impedance results in a gain shoot at the resonance frequency (Fig. 8.e), it can be compensated by increasing the DC gain. The transient simulation is done for a full-scale sinusoidal input at 10^8 MHz combined with a periodic pulse (Fig. 8.f). The required current for the charge and discharge of the anti-resonance cancellation paths are correctly provided (Fig. 8.(a,b)). However, the current peaks result almost certainly in saturating the following stage and they must be removed at the output of the LWR. The current peaks are in common-mode between the positive and the negative outputs and can be eliminated by a differential system (buffer$_2$).

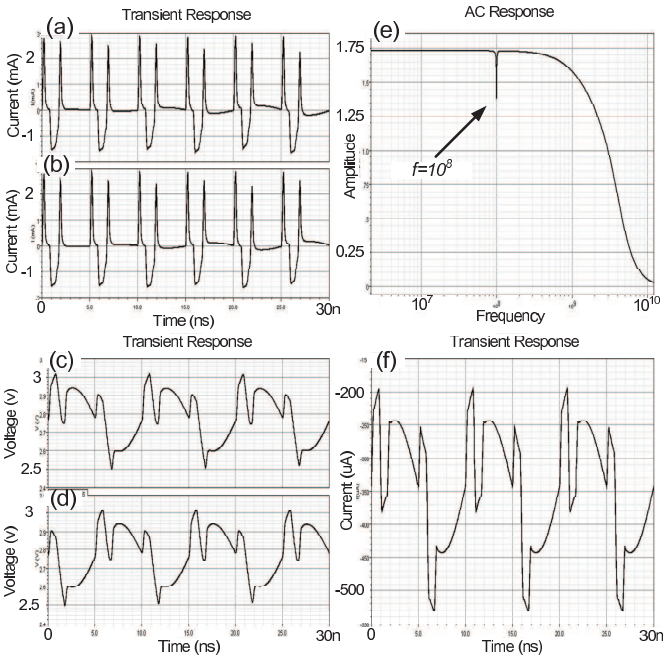

Fig. 8. The positive (a) and the negative (b) LWR output current, the positive (c) and the negative (d) LWR driving voltage , the AC response of buffer$_1$ (e) and the buffer$_1$ input current (f).

The schematic of the buffer$_2$ cell is shown in Fig.9.a. The first stage is a common-base arrange (T_3) able to provide a low input impedance depending on its bias current. An n-mode current mirror (M_{11} and M_{12}) and a p-mode current mirror (M_8 and M_9) are used to creat two inverse current. The current path, providing I_{out-}, includes three transistors (M_{10}, M_{11} and M_{12}) while that of I_{out+} includes only one transistor (M_9). As a result, I_{out-} has a phase delay compared with I_{out+}. R_4 must be optimized to make them symmetric. The global view of the differential buffer is shown in Fig.9.b. I_{out+} of the negative path is in differential mode with I_{out-} of the positive path. Adding them not only results in eliminating the common-mode peaks, but also the bias current of T_3 is removed.

IV. Layout Results

The performance of the proposed circuits depends on the differential functionality. The errors produced because of mis-match in differential-mode result in deteriorating the resonator performance. Therefore, strict considerations are taken into account for the layout design. The arrange of the devices must be optimal to reduce the parasite capacitances because of the presence of high frequency signals. Moreover, the symmetry between the differential pairs must be respected. This means the same distance from heat sources, the same

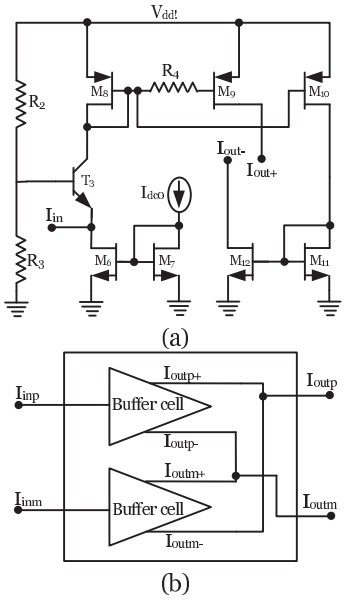

Fig. 9. The proposed schematic for buffer$_2$ cell (a) and the global view of buffer$_2$.

width and length of the paired analog devices (like transistors and resistors) and the same pathway of metal tracks. Fig. 10 shows the layout of buffer$_2$. The electronic control circuit loaded by LWR is simulated at layout-level. Fig. 11.a is the positive and the negative output currents for an input current shown in Fig. 8.(f). Also, the performance of the circuit for a pure sinusoidal input current is shown in Fig.11.b.

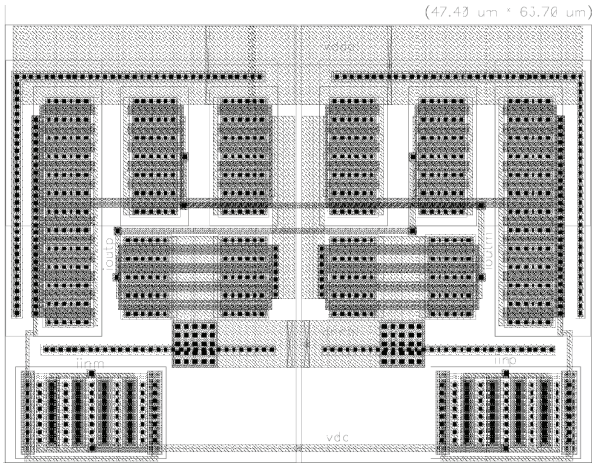

Fig. 10. The layout of the second buffer.

This structure was tested in the context of a 6^{th}-order single-stage feed-forward band-pass CT $\Sigma\Delta$ modulator based on LWR and the results are satisfying.

V. Conclusion

In order to ensure the performance of a high-order classical wide-band $\Sigma\Delta$ modulator, the used resonator must be able to perform a Q-factor around 100 with an accurate resonance

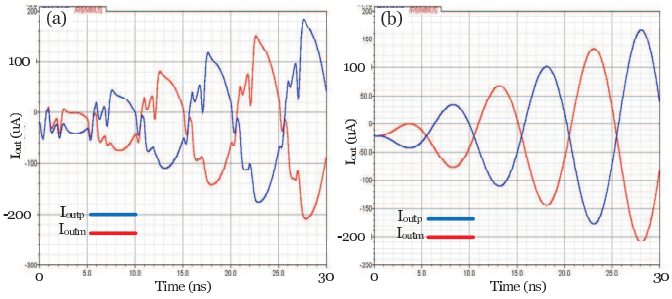

Fig. 11. The positive and the negative output currents (a) for an input current shown in Fig. 8.f and the performance of the circuit for a pure sinusoidal input current (b) of the electronic control circuit loaded by LWR simulated in layout-level.

frequency. Although the required characteristics are achievable by piezo-electric resonators, their performance suffers from impedance adaptation mismatch and anti-resonance frequency. An electronic control circuit is proposed to overcome the issues. Low input or output impedance, the ability of providing a large charge and discharge current and anti-resonance cancellation are the specifications of the proposed circuit. The electronic control circuit has been designed in AMS Bi-CMOS $0.35\mu m$ offering npn-BJT transistors. The simulation results, at layout-level, proves the reliability of the proposed solutions.

References

[1] P. Benabes, A. Beydoun and J. Oksman, *Extended Frequency-Band-Decomposition Sigma-Delta A/D Converter*, SpringerLink Journal on Analog Integrated Circuits and Signal Processing, vol. 61, issue 1, October 2009.

[2] R. Yu and Y. Xu, *Band-Pass Sigma-Delta Modulator Employing SAW Resonator as Loop Filter*, IEEE Transactions on Circuits and Systems I, vol.54, issue 4, pp. 723-735, April 2007.

[3] K. Reddy and S. Pavan, *Fundamental Limitations of Continuous-Time DeltaSigma Modulators Due to Clock Jitter*, IEEE Transactions on Circuits and Systems I, vol. 54, issue 10, pp. 2184-2194, October 2007.

[4] S. Norsworthy, R. Schreier, G. Temes, *Delta Sigma Data Converters: Theory, Design and Simulation*, Handbook, Wiley-IEEE Press, October 1996.

[5] M. Javidan and P. Benabes, *A New Method to Synthesize and Optimize Band-Pass Delta-Sigma Modulators for Parallel Converters*, IEEE International Workshop on Circuits and Systems and TAISA Conference conference, pp. 197-200, June 2008.

[6] B. Xia, S. Yan and E.S. Sinencio, *An RC Time Constant Auto-Tuning Structure for High Linearity Continuous-Time Sigma-Delta Modulators and Active Filters*, IEEE Transactions on Circuits and Systems I, vol.51, issue 11, pp. 2179-2188, November 2004.

[7] H. P. Loebl, C. Metzmacher, D. N. Peligrad, R. Mauczok, M. Klee, W. Brand, R. F. Milsorn, P. Lok, R. Van Straten, A. Tuinhout and J. W. Lobeek, *Solidly Mounted Bulk Acoustic Wave Filters for the GHz Frequency Range*, IEEE International Conference on Ultrasonics, pp. 919-923, October 2002.

[8] M. Desvergne, C. Bernier, P. Vincent, Y. Deval and J. B. Begueret, *Intermediate Frequency Lamb Wave Resonators and Filters for RF Receiver Architectures*, IEEE International Conference on Electronics Circuits and Systems, vol. 10, issue 13, pp. 1045-1048, December 2006.