Fixed-step Simulation of Continuous-Time sigma-delta Modulators

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***Abstract*— A methodology for the simulation of Continuous Time Sigma-Delta (CTΣΔ) converters is presented in this paper. This method permits the simulation of ΣΔ modulators employing continuous-time filters using a fixed-step algorithm. The analysis method is based on the discretization of a continuous-time model and using a discrete simulator, which is more efficient than an analog simulator. In our analysis approach, each sampling-period is divided into a fixed number of steps. This transformation is exact in term of Noise Transfer Function and asymptotically exact in term of Signal Transfer Function (the Signal Transfer Function of the model rapidly tends to the continuous time model transfer function when the number of steps increases). Moreover, the ideal step-size can be estimated from the bandwidth of the input signal.**

I. INTRODUCTION

Discrete Time Sigma-Delta (DTΣΔ) circuits are very attractive analog-to-digital converters because they achieve high accuracy with few critical analog components [1]-[2]. They are composed of a ΣΔ modulator which provides a high speed one bit data string followed by a digital filter and decimator to produce a high resolution data. Unfortunately, the speed of these circuits is limited. Using switched-capacitors technologies, the sampling frequency of the modulator is limited by a few tenth of MHz which results in a signal bandwidth between 50 kHz and a few MHz.

An alternative to the use of Discrete-Time (DT) filters is the use of Continuous-Time (CT) filters [3][4]. Although CT filters are not easy to integrate, they possess one key advantage over their discrete-time competitors: no sampling is performed within the filter itself. As a first result, the restriction of the mentioned maximum sampling frequency is removed. Secondly, both sampling errors and out-of-band signals which alias into the bandpass are reduced by the high gain of the forward loop in the bandpass. On the other hand, continuous-time circuits are more difficult to design and to simulate than discrete-time circuits.

When simulations are done by an analog simulator, it takes a huge computational time. Equivalent discrete-time model of CT modulator loop have been described [5][6], but they need a continuous filter in the input signal path to ensure the exact equivalency, and furthermore the input bandwidth is limited to half the sampling frequency.

In this paper, an analysis method of CT modulators based on Oversampled Discrete Time (ODT) models is presented. With this method, each sampling-period is divided into a fixed number of steps. We will show that this transformation is exact in term of Noise Transfer Function (NTF) and asymptotically exact in term of Signal Transfer Function (STF). The STF of the model rapidly tends to the STF of the CT model when the number of steps increases. Besides, an estimation of the ideal step-size from the bandwidth of the input signal will be performed.

This paper is structured as follows. The following section describes the synthesis and analysis method of continuous filter ΣΔ modulators. An application of a second order modulator is illustrated in Section III. Finally, concluding remarks are given in Section IV.

II. SIMULATION METHOD OF CONTINUOUS FILTER ΣΔ MODULATORS

A. *Equivalency between Continuous-Time and Discrete-Time Filters*

The behavior of ΣΔ modulators employing CT filters has been widely studied for ten years, especially high order stable topologies. Directly designing and optimizing a CT modulator can take a very long time if only an analog simulator is used. A better solution is to design and to optimize a ΣΔ modulator with discrete-time filters and transform it by a mathematical tool into a continuous-time ΣΔ modulator.

The relationship between the CT filter transfer function ($g(s)$) and the DT transfer function ($f(z)$) can be expressed using the formula [5],

$$f(z) = (1 - z^{-1}) \mathrm{Z}_T \left\{ L^{-1} \left[\frac{g(s)}{s} \right] \right\} \qquad (1)$$

when the loop delay can be neglected. This formula ensures the equivalency of the NTF between CT and DT topology as shown in Figure 1.

Extra loop delay could be taken into account [5], but in order to simplify the discussion, it will be neglected here.

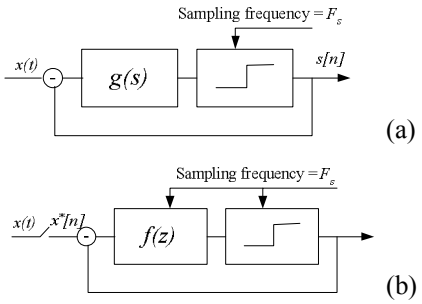


Figure 1 : Single-bit CT (a) and DT modulator (b).

Assuming that the input signal is a band-limited signal (limited to the half of the sampling frequency), and that the quantizer can be modeled by an additive white noise, the signal transfer function of the discrete-time topology can be expressed as :

$$STF_{DT}(\varphi) = \frac{f(e^{2j\pi\frac{\varphi}{F_S}})}{1+f(e^{2j\pi\frac{\varphi}{F_S}})} \qquad (2)$$

where F_s is the sampling frequency.

The signal transfer function of the continuous-time topology is $STF_{CT}(\varphi) = \frac{g(2j\pi\varphi)}{1+f(e^{2j\pi\frac{\varphi}{F_S}})}$ (3)

f being related to g by equation (1).

Figure 2 shows the modulus of the DT and CT STF for a first-order lowpass modulator. It can be clearly seen that these transfer functions differ for non null frequencies which means that any simulation performed for a non constant signal will be wrong using the discrete model, especially for high frequencies.

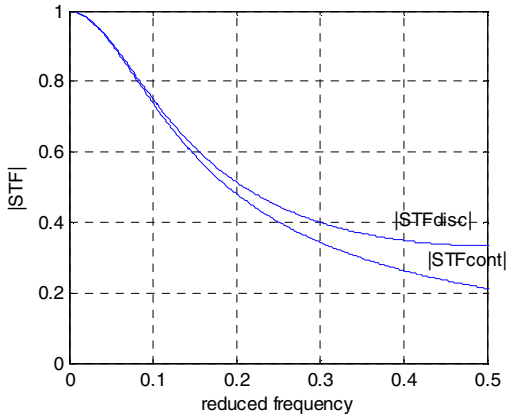


Figure 2 : STF for a CT and DT modulator.

Furthermore, the discrete-time model is unable to model an input signal with a frequency higher that half the sampling frequency.

In order to enhance the signal-transfer function and remove the frequency limitation, we propose to use an oversampled model of the discrete-time modulator (ODT).

B. Oversampled model of a sigma delta modulator

Let's consider now the oversampled model of a ΣΔ modulator. The sampling frequency of the ADC is still F_s, but the digital filter F(z) runs now at kF_s. The feedback signal is held during k samples. In order to simplify the notations, the Z variable denotes functions running at frequency kF_s, while the z variable denotes a function running at frequency F_s.

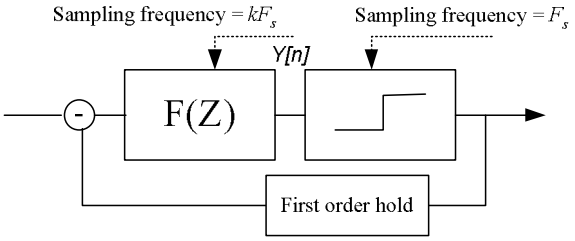


Figure 3 : Oversampled modulator.

Now we consider the transfer function between the ADC output and its input. We calculate the response to a discrete impulse ($Y^*[n]$) in the three cases: discrete-time modulator, continuous-time modulator, and oversampled discrete-time modulator (T is the sampling period).

Table I gives equivalency between DT, CT and ODT modulators for first order, second order and third order integrators, by identifying the impulse responses $Y^*[n]$. These formula were obtained using Maple software.

	$g(s)$	$f(z)$	$F(Z)$
First order Integrator	$\frac{1}{s}$	$\frac{z^{-1}}{1-z^{-1}}$	$\frac{1}{k}\frac{z^{-1}}{1-z^{-1}}$
Second-order integrator	$\frac{1}{s^2}$	$\frac{1}{2}\frac{(z^{-1}+z^{-2})}{(1-z^{-1})^2}$	$\frac{1}{2k^2}\frac{(z^{-1}+z^{-2})}{(1-z^{-1})^2}$
Third order integrator	$\frac{1}{s^3}$	$\frac{(z^{-1}+4z^{-2}+z^{-3})}{6(1-z^{-1})^3}$	$\frac{(z^{-1}+4z^{-2}+z^{-3})}{6k^3(1-z^{-1})^3}$

TABLE I. EQUIVALENCIES BETWEEN CT, DT, AND ODT

In the case of the DT modulator : $Y^*[n] = \mathrm{Z}^{-1}\left(f(z)\right)$ (4)

In the case of the CT modulator :

$$Y^*[n] = L^{-1}{}_{t=nT}\left[\frac{1-e^{-Ts}}{s}g(s)\right] \qquad (5)$$

In the case of the ODT modulator :

$$Y^*[n] = \mathrm{Z}^{-1}{}_{N=kn}\left[\frac{1-Z^{-k}}{k(1-Z^{-1})}F(Z)\right] \qquad (6)$$

It can be noticed that the DT case is a particular case of the ODT modulator for k=1, and the CT case can be seen as the limit when k tends to infinity of the ODT model.

III. Application to the Simulation of a Second-Order ΣΔ Modulator

A. Oversampled model of a sigma delta modulator

High order ΣΔ modulators employing DT filters have been widely studied. Most of them are designed with multiple-loop topologies. Usually CT topologies are derived from their DT counterpoint using table 1 transformation formulas. We consider a classical second-order modulator (Figure 4) [7]. The CT equivalent modulator is given by Figure 5 using the methodology of [5]. For this purpose, the ADC input has been first decomposed to the sum of the output signals of filters whose inputs are sampled and held. Then each discrete-time integrator has been replaced by its continuous-time equivalent filter thanks to Table I. The elements of this modulator have then recombined to give the usual modulator structure (Figure 5).

It must be noticed that the equivalency is only exact for the NTF. The STF has not been taken into account in this transform.

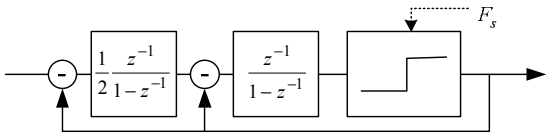


Figure 4 : DT modulator.

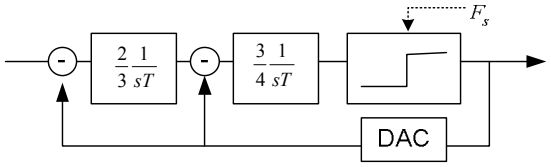


Figure 5 : CT equivalent modulator.

In order to simulate the CT modulator, we use the same methodology to transform the CT modulator into an ODT topology. This operation takes into account the feedback signal and the input signal of the modulator. A pre-distortion FIR filter (d(Z)) has been introduced to compensate the error introduced by replacing the CT filter from the signal input to the ADC input ($g(s)$) by the ODT filter. In the case of a second order integrator, it can be expressed as:

$$d(Z) \approx 0.09 + 0.82Z^{-1} + 0.09Z^{-2} \qquad (7)$$

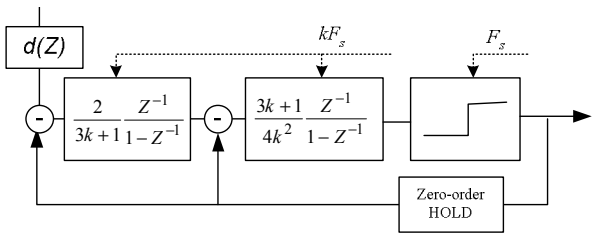


Figure 6 : Equivalent ODT modulator.

The transformation's result topology is presented in Figure 6. When k tends to infinity, the ODT tends to the CT one in terms of STF and NTF.

B. Signal transfer function evaluation

The STF of a second-order modulator was evaluated (still by making the assumption that the quantization noise behaves as an additive white noise) using the ODT model. In order to evaluate the efficiency of our methodology, this STF is compared with the one that would be obtained by making a Bilinear Transform (ODTbt) of the filters of the CT modulator (Figure 7 topology). One must notice that this topology is not strictly equivalent in term of NTF.

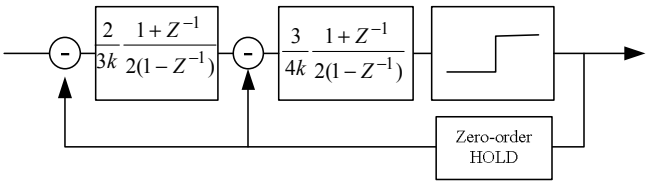


Figure 7 : ODT equivalent model obtained by a bilinear transform.

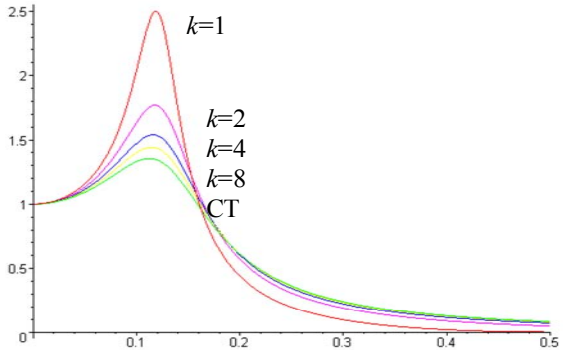
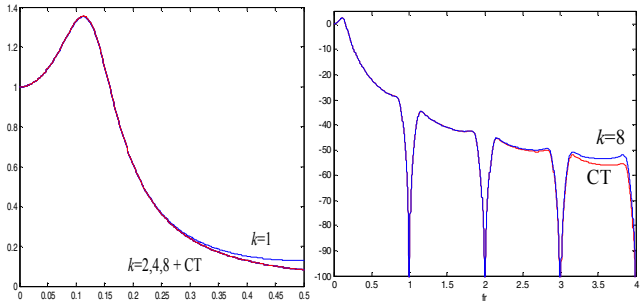


Figure 8 : |STF| for k=1, 2, 4, 8 for the ODTbt modulator compared with the CT modulator



(a) (b)

Figure 9 : |STF| for k=1, 2, 4, 8 for the ODT modulator and the CT modulator within (a) and outside (b) the band

The modulus of the STF of the model obtained by bilinear transform (ODTbt) is given in Figure 8 and the one of the ODT modulator is given in Figure 9(a). With a classical bilinear transform, the STF remains far from the real STF even for large k. Using the ODT, the STF is near from the real STF even for low k values. The phases curves have not been plotted but phases are also accurate for the ODT model.

The ODT model allows applying input signals from 0 to $kF_s/2$. The STF can be extended to frequencies higher than $F_s/2$ using the convention that a signal at frequency $\phi+mF_s$ is aliased into a term at frequency ϕ at the modulator input. Figure 9(b) compares the STF of the CT modulator and ODT for k=8 at frequencies higher than $F_s/2$. The obtained STF is very accurate from 0 to the sampling frequency. We verified, by plotting the modulus of the STF for first order, second order, and third order topologies for several k values, that taking k equal to four times the ratio between the input-signal bandwidth and *Fs/2* is accurate.

C. *Simulation results*

The three modulators have been simulated using Simulink. We verify by simulations that they are equivalent in term of NTF. Figure 10 shows a time domain simulation for a constant input signal of the second-order modulator. The three curves represent the ADC input signal for the DT, CT and ODT case. It can be seen that the three signals are equal at the sampling times nT. Furthermore the CT and ODT signals are equal for each nT/k time, showing that the ODT model response tends to the CT model when k tends to infinity.

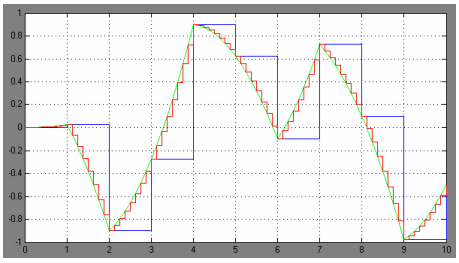


Figure 10 : Time domain simulations of the ADC input signal for CT, DT and ODT modulator.

We have then applied a sum of sine signal (reduced frequencies are 0.025 0.05 0.075 0.1 0.125 0.15 0.6 & 1.5). Figure 11 gives the output Power Spectral Density (PSD) obtained with the DT model. The aliased components are clearly bad. Figure 12 compares simulation results between the CT and ODT model. The in-band and aliased terms are correctly calculated by the ODT model

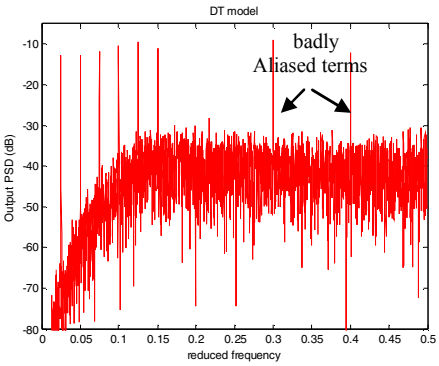


Figure 11 : PSD of the DT model.

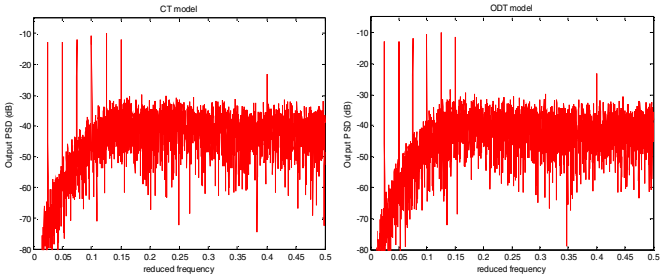


Figure 12 : PSD of the output signal with CT & ODT model.

Table II compares the simulations times in simulink (100000 samples) of the proposed simulation methods.

	continuous	D.T.	Bilinear (k=8)	Bilinear (k=128)	ODT (k=8)
Simulation time	34s	1s	6s	130s	6s

TABLE II. SIMULATION TIMES

The discrete-time model is the fastest one but is not good in term of STF. The continuous-time model is quite slow. The best compromise is found by using the ODT model which is 6 times faster that the CT one

IV. CONCLUSIONS

A new methodology for time-domain simulations of CT modulators is proposed. This methodology is based on a fixed step discretization of each output sample. Using this method, simulations are very fast as they use a fixed step algorithm and discretized equations. STF considerations on a second-order modulator have shown that the ODT method describes the behavior of a CT modulator better than classical transform method such as bilinear transform. Besides, we have checked that this methodology can be extended to the case of bandpass modulators but the results could not fit into this paper.

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