A Sigma-Delta Converter with Adjustable Tradeoff between Resolution and Consumption

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Abstract — **This paper proposes an analog-to-digital converter with two working modes. In the first mode, the system is a sigma-delta passive converter: the analog modulator uses a passive switched-capacitor low-pass filter and the only active element is the comparator. The consumption is low and the resolution is moderate (9 bits). In the second mode, the expected resolution is 15 bits. For that, the passive sigma-delta modulator is put in a loop with a low-pass amplifier and some digital processing elements. The principle of this two-mode system is validated by functional simulations and by the test of a circuit realized in a 0.35µm CMOS technology.**

I. INTRODUCTION

Passive sigma-delta (ΣΔ) analog-to-digital modulators [1, 2] are a very attractive way to build very-low consumption analog to digital (A/D) converters. In these modulators, the active low-pass filters which are generally used for sigma-delta conversion are replaced by passive ones. The only active element is a one-bit comparator working as an A/D converter.

The main advantage of such an approach is the very low consumption of the analog part of the converter. However, the resolution and the bandwidth are limited. For these reasons, the applications of passive sigma-delta conversion are essentially the monitoring of steady signals. It has to be noticed that the non-linearity error caused by the passive modulator is high and has to be digitally corrected, which means that the modulator has to be calibrated.

We are proposing in this paper a new conversion system which uses a passive sigma-delta modulator and has two possible working modes. In the "low consumption mode" (also named "passive mode"), the modulator is simply followed with a low-pass digital filter which also decimates the signal. The expected resolution is then 9 bits. In the "high resolution mode" (also named "active mode"), the modulator is inserted in a loop with an active low-pass filter and digital functions. The expected resolution is then 15 bits. The active mode can be used for example to calibrate the passive modulator.

In this paper, we are first presenting the principle of this two-mode topology (II) and some high-level simulation results (III). Then, the circuit realized to validate this principle and to investigate the limitations is described (IV). Finally, some measurement results are presented (V).

II. HIGH-LEVEL TOPOLOGIES

A. Passive modulator

The design of a passive low-pass discrete-time second-order sigma-delta modulator has already been presented [3]. The architecture consists of a single loop (Fig. 1) and is calculated from the MSCL (Multi Stage Closed Loop [4]) architecture shown in Fig. 2.

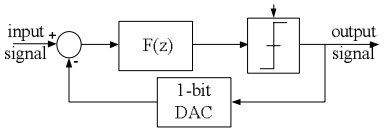

Figure 1. Sigma-delta single-loop modulator

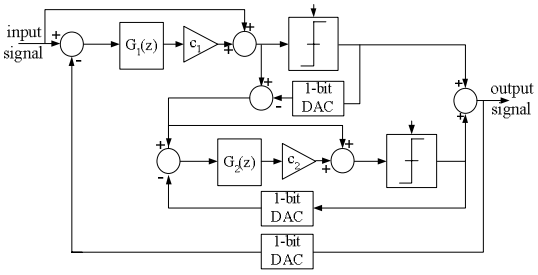

Figure 2. Sigma-delta second-order MSCL modulator

The transfer functions $G_j(z)$ should be integrators. Due to some physical limitations, they behave generally as low-pass active filters and can be written by using their Q-factor (which is the inverse of their cutoff frequency):

$$G_j(z) = \frac{Q_j}{Q_j + 1} \frac{z^{-1}}{1 - \frac{Q_j}{Q_j + 1} z^{-1}} \quad (1)$$

As shown in [4], the MSCL architecture is equivalent to the single-loop architecture with *F(z)* given by formula (2): :

$$F(z) = \prod_{j=1}^{order=2} \left(1 + c_j G_j(z)\right) - 1 \qquad (2)$$

In our case, the loop filter is passive, therefore its gain must be equal to 0 dB for a null frequency. Formula (3) is adjusted to satisfy this requirement:

$$F(z) = \frac{\prod_{j=1}^{order=2} \left(1 + c_j \frac{Q_j}{Q_j+1} \frac{z^{-1}}{1 - \frac{Q_j}{Q_j+1} z^{-1}}\right) - 1}{\prod_{j=1}^{ordre=2} (1 + c_j Q_j) - 1}. \qquad (3)$$

Formula (3) exhibits several degrees of freedom: coefficients Q_j and coefficients c_j. Some high-level simulations were performed to analyze their effect on the modulator performances (resolution, stability) and on the signal level at the comparator input. We showed [3] that a good compromise for a second-order structure can be found with:

$$c_1 = c_2 = 0.5,\ Q_1 = 10 \text{ et } Q_2 = 50 \qquad (4)$$

With these values, the expected theoretical resolution for an over-sampling ratio of 100 is about 9 bits. The comparator input is about 10 mV, compatible with low-consumption electronics.

B. Active topology principle

The passive modulator causes a high non-linearity error when the input signal is far from the full scale mid-point. The principle of active topologies is to insert the modulator in a loop in order to keep its input signal closed to the mid-point. This principle is illustrated by Fig. 3.

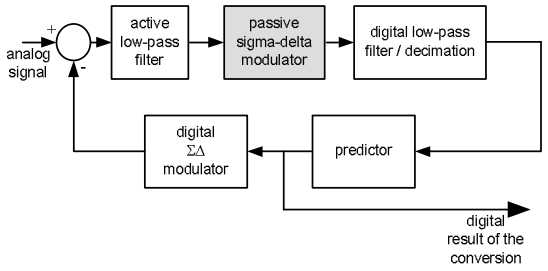

Figure 3. Active simple topology

The analog part of the converter is composed with an active low-pass filter and the passive modulator. The digital part is composed with a digital low-pass filter, which also decimates the signal, a predictor and a D/A sigma-delta modulator. The predictor estimates the value of the input signal at the current time from the samples delivered by the digital filter. This predictor can be a simple integrator (with a gain lower than 1 in order to ensure the stability of the loop). After crossing the D/A modulator, the prediction is subtracted from the input signal. The active low-pass filter reduces the quantization noise introduced by the D/A ΣΔ modulator.

The delay introduced by the digital filter increases the response time of the closed loop. Consequently, this topology is well suited only for slow signals. In order to get a faster response time, a new digital processing is proposed (Fig. 4). The digital filter has been divided into two parts. The first part reduces the quantization noise without introducing a too large delay. Elements (E) and (F) are digital models of the analog part. They help increase the response speed and the bandwidth of the converter. They should be matched with the analog part as well as possible.

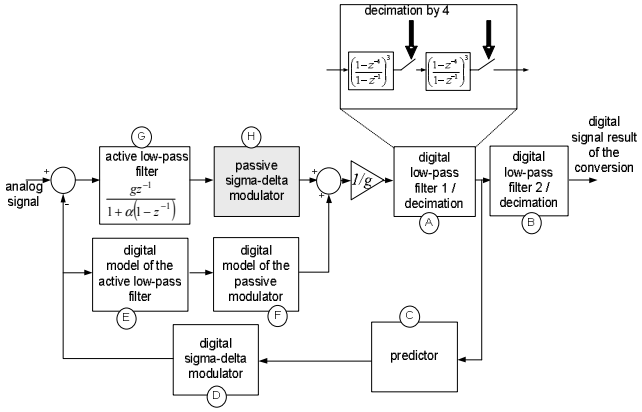

Figure 4. Active fast topology

III. HIGH-LEVEL SIMULATION RESULTS

A. Linearity and resolution

Some transient simulations with a static input signal were performed in order to evaluate the expected linearity and resolution. Two converter configurations were compared:

- in passive mode : passive modulator followed with digital filters 1 and 2 (A and B in Fig. 4) ;
- in active mode : active fast topology as shown in Fig. 4 ; for the active filter, the gain g is taken equal to 8 and α to 40 ; digital parts E and F are supposed fully matched to analog ones (G and H) ; the predictor (C) is a linear interpolator.

In both cases, the over-sampling ratio is equal to 256 and the sampling frequency is 8 MHz.

Fig. 5 shows the converter output as a function of time in passive and active modes. The DC input signal is taken equal to -0.5 (the full scale here is normalized between -1 and 1). The mean output value in passive mode is -0.4972 (non-linearity error – difference between the input value and the output mean value – equivalent to a resolution of 9.5 bits) whereas it is -0.49998 in active mode (non-linearity error equivalent to a resolution of 16.6 bits). Besides, the precision can be calculated from the residual noise at the output and expressed in bits. It is about 12.3 bits in passive

mode and 15.5 bits in active mode. The linearity is enhanced by 7 bits in active mode and the precision by 3 bits.

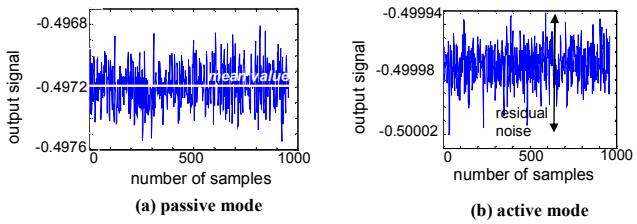

Figure 5. Converter transient response for a static input equal to -0.5

Fig. 6 shows the non-linearity error as a function of the DC input value. The input signal is rescaled between -1 and 1. Fig. 6(a) is obtained after a first-order gain correction. It can be clearly seen that the modulator is highly non-linear for the extreme input values. Fig. 6(b) demonstrates the benefit of the active topology. It is obtained without any post-correction. We get a theoretical rail-to-rail conversion with a very linear DC transfer function: the non-linearity error is kept below 2×10^{-5} on the whole input range (equivalent to a resolution of 16.6 bits). The quantization noise becomes the predominant error source.

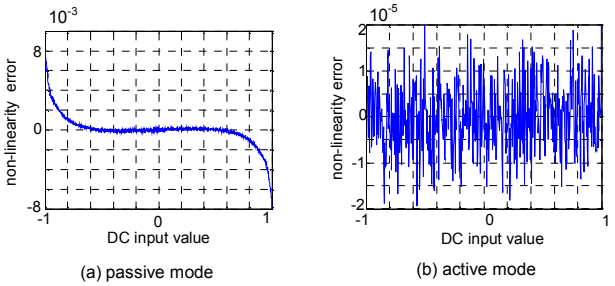

Figure 6. Non-linearity error in passive and active modes

B. *Bandwidth*

Some simulations were performed with sinus input signals in order to compare the bandwidth of the simple and fast active topologies. Fig. 7 shows the transient response of the simple topology when the input frequency is 20kHz and the sampling frequency is 10MHz. The gain is below 0.3. The same simulation with the fast active topology gives a gain above 0.8.

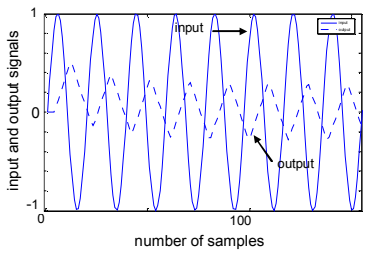

Figure 7. Transient simulation with a sinus input signal (f_{input} = 20kHz ; $f_{sampling}$ = 10MHz)

IV. CIRCUIT AND PHYSICAL DESIGN

A prototype circuit was realized in order to validate the principle of the two-mode topologies and to investigate the limitations.

The digital part (A to F in Fig. 4) was defined as a HDL code and implemented in an Altera board whereas the analog parts (G and H) were integrated in the AMS 0.35µm technology. The chip is composed with:

- the comparator ;
- the passive switched-capacitor filter ;
- the active switched-capacitor filter ;
- the $V_{DD}/2$ reference generators (virtual ground) where V_{DD} is the supply voltage ;
- a digital part using standard cells (essentially switches command).

The comparator, the passive filter and the reference generators were presented in the article [5]. As far as the active filter is concerned, regarding our objectives (validation and investigation), the choice criterion was simplicity. Consequently, the circuit (Fig. 8) is single-ended and there is only one capacitor at the input.

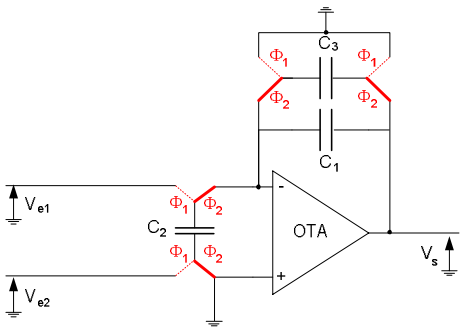

Figure 8. Switched-capacitor active filter

The transfer function is:

$$\frac{V_S}{(V_{e_1}-V_{e_2})}=\frac{-\frac{C_2}{C_3}z^{-1}}{1-\frac{C_1}{C_3}\left(1-z^{-1}\right)} \qquad (5)$$

V_{e1} is the input signal to convert and V_{e2} *is* the feedback signal (delivered by the digital sigma-delta modulator). As V_{e2} is a binary signal, this input is connected to the ground or to the V_{DD} supply by adequate switches. The signal reference (represented by a virtual ground in Fig. 8) is $V_{DD}/2$. It is produced by a switched-capacitor voltage divider.

This amplifier can be bypassed when the passive mode is used. In this case, the biasing sources of the operational amplifier are switched off, in order to reduce the global consumption.

The chip layout is shown in Fig. 9. All the components are duplicated for test purpose.

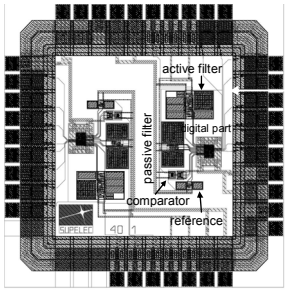

Figure 9. Chip layout

V. MEASUREMENT RESULTS

A. Linearity

The tested configurations are the same than the ones described in III.A. The supply voltage is 3.3 V. The measurement precision of the input voltage is about 0.1%. In active mode, the digital parts (E and F) are calibrated so that they are fully matched with the analog parts (G and H).

Fig. 10 gives the non-linearity error as a function of the DC input value (normalized between 0 and 1) in passive and active (fast topology) modes. Offset and gain error have already been compensated. In passive mode, the non-linearity error is below 1.5×10^{-3} in the range [0.1 ; 0.9], which corresponds to an equivalent resolution of 9.3 bits. In active mode, it is below 4×10^{-4} in the range [0.1 ; 0.7] which corresponds to an equivalent resolution of 11.3 bits. The non-linearity increases drastically above 0.7.

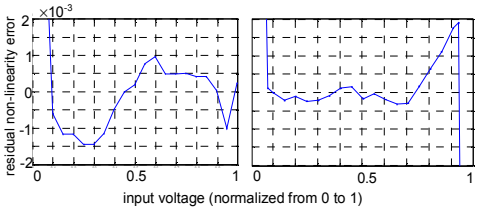

Figure 10. Non-linearity measurement

Thus, the linearity is the one expected in passive mode, but it is far lower than expected in active mode. Besides, the conversion is not rail-to-rail. Further high-level and transistor simulations, which are not presented here, have demonstrated that this is due to the active filter: its common-mode rejection is not high enough (about 32 dB) and the common-mode gain is deeply non-linear.

B. Precision

The precision is calculated from the residual noise at the output for a DC input. It is 9.6 bits in passive mode and 12.3 bits in active fast mode. Thus, in passive mode, it is lower than expected with high level simulations (9.5 bits measured instead of 12.3 bits expected). The reasons are:

- charge injection effects ;
- sensitivity to digital noise in the analogue part (due to the low amplitude of the comparator input)

There are 2.5 bits of difference between the active and the passive modes (3 bits were expected).

C. Bandwidth

The measured bandwidth in active fast mode is about 15 kHz, which is compatible with audio applications.

D. Consumption

The measured consumption for F_s = 1MHz is 1.4 µA for the passive modulator and 173 µA for the input active filter. The consumption of the digital part on the Altera board can not be measured.

VI. CONCLUSION

This paper proposes a new conversion system based on passive sigma-delta modulation, which offers two working modes: the "low consumption" (passive) mode and the "high resolution" (active) mode. Measurements validate the principle demonstrated at the functional level and point out some limitations. The experimental resolution is 8 bits in passive mode (passive modulator followed by a digital filter) with the use of a digital post-correction. The measured analogue consumption is lower than 2µA at a 1 MHz data rate. In active mode, the modulator is inserted in a loop composed with an active filter and some digital functions. The resolution should theoretically be increased by 6 bits but it is only by 2.7 bits experimentally. This could be enhanced by redesigning the active filter (use of full differential circuits and bottom-plate technique). We are investigating through high-level simulations the effect of the predictor and active filter parameters, and of the mismatch between digital models and their analogue counterparts.

VII. ACKNOWLEDGEMENTS

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