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Abstract—A robust and hardware efficient dynamic element matching (DEM) algorithm is developed and used to design a $2^3$-order bandpass (BP) mismatch-shaping circuit, moved inside the feedback loop of a $6^{th}$-order bandpass continuous-time delta-sigma modulator. This algorithm is based on a shortened tree-structured scheme (STDEM) which can assure a stable high order mismatch-shaping with a modest circuit volume. The modulator has a 3-bit quantizer and 8 thermometric feedback DAC’s cells. The designed DEM’s circuits is simulated in 0.35µ-CMOS which can be clocked up to 300-MHz. The mismatch error floor is decreased of about 35dB in the band of interest. Its related circuit occupies of about 0.22mm$^2$ area.

I. INTRODUCTION

With increasing demand of ΔΣ modulators (DSMs) with broader bandwidth and wider dynamic range (DR), multibit architectures become attractive for this trend as [1], [2]:

- the SNR directly increases by 6dB for each extra quantization bit, resulting in lower OSR application possible,
- multibit DSM’s loop possesses better stability resulting in additional loop gain for higher order structure, which in turn results indirectly in improved SNR,
- it is one of the best ways to reduce clock jitter noise resulting in high frequency application possible,
- it possesses lower idle tone and lower out of band noise,
- in multibit DSM, the first opamp needs lower input range and slew-rate resulting in lower power consumption.

On the other hand, a multibit DSM needs a multibit-DAC on the feedback path which is usually a thermometric current steering DAC limited to 5-bits. Any feedback-DAC can suffer from inevitable mismatching occurred during fabrication process. This is a large disadvantage of the multibit DAC which seriously degrades its $SNR$, as it acts in the feedback path. Multibit architecture has no other sever inconvenience and its circuits’ complexity can be accepted if one needs such many advantages mentioned above.

In order to integrate a multibit DSM, several error correction methods have been developed as trimming, calibration, digital correction, and dynamic element matching (DEM). The last one is widely used in high performance integrated modulators having a resolution over 10 bits. This technique can be realized in different ways. Randomization scheme whitens DAC’s mismatch errors over whole frequency range, so that input depended tones are diminished but its noise floor increases in the band of interest. Thus, better solution can be using a mismatch noise shaping technique. The well-known data weighted averaging method (DWA) can effectively be used to shape mismatch errors reside in signal band. However, with the same frequency as in the quantizer, it can mainly be applied as a first order lowpass mismatch-shaping. For higher order mismatch-shaping error, only two original methods have been introduced; feedback-vector or sorting algorithm (SDEM) [3] and tree-structured scheme (TDEM) [4]. The SDEM suffers from lower hardware efficiency and clock rate limits, especially for higher number of quantization level. The TDEM suffers more from algorithm instability for high order mismatch-shaping.

The authors have lately developed two new schemes, which are based on two mentioned original methods. The first one, called MDEM, is a mixed structured of SDEM and TDEM [5]. The MDEM benefits of better stability nature of SDEM and hardware efficiency of TDEM. The second one, called STDEM, is a shortened tree-structured introduced in [6]. It is more stable than the pure TDEM with the same hardware efficiency. This paper tends to further illustrate the STDEM algorithm and introduces its related circuits, which are designed for a 3-bit feedback-DAC, in two next sections.

II. SHORTENED TREE-STRUCTURE DEM (STDEM)

STDEM algorithm is based on conventional TDEM [4], [6]. Fig.1 shows an example of a 9-level TDEM (on the left) and its equivalent STDEM (on the right). These two algorithms have two main differences, which results in a better performance for STDEM. Each group of the last three blocks in TDEM structure is replaced by an Ending Switching Block (ESB) to obtain a STDEM structure. In addition, the remaining switching blocks in STDEM will act in different way from that of TDEM. Some more details of STDEM will be developed here in the below.

Generally, a $(1+2^B)$-level TDEM consists of $B$ layers shown...
as $B$ different columns (see a 3-bit example in Fig.1–a). Each $k^{th}$-layer can also consist of $2^{(B-k)}$ boxes laid out in rows. All boxes within the tree structure are called switching blocks (SB), are labeled $S_{kr}$, where $k$ denotes the layer number and $r$ denotes its position in the layer. Each $S_{kr}$ has a $(k+1)$-bit input $y_{kr}$ and two $k$-bit output: $y_{k-1,2r-1} = (y_{kr} + S_{kr})/2$ and $y_{k-1,2r} = (y_{kr} - S_{kr})/2$. Also, $S_{kr}(n)$ must satisfy certain conditions for number conservation rule, as:

$$S_{kr}(n) = \begin{cases} \text{even if } y_{kr} \text{ is even} \\ \text{odd if } y_{kr} \text{ is odd} \end{cases}$$

\[ |S_{kr}(n)| \leq \min\{y_{kr}(n), 2^k - y_{kr}(n)\} \quad (1) \]

![Fig. 2. a)Conventional SB’s structure b)switching sequence generator](image)

This definition imposes a very strict rule to produce $S_{kr}(n)$ sequences so that it takes only zero for any even SB’s inputs. This in turn, can cause instability in the mismatch shaping loop and overflow can occur in the second and following stages of the filter if the input of the SB is even for a few periods. To meet better stability, it was then modified [7]:

$$S_{kr}(n) = \begin{cases} +1 & y_{kr} \text{ is odd and } V_{kr} > 0 \\ -1 & y_{kr} \text{ is odd and } V_{kr} < 0 \\ +2 & y_{kr} \text{ is divisible by } 4 \text{ and } V_{kr} > 0 \\ -2 & y_{kr} \text{ is divisible by } 4 \text{ and } V_{kr} < 0 \\ 0 & \text{in all other cases} \end{cases}$$

(2)

The above-mentioned modification results in better stability, but it is not sufficient and a further restriction must be added to maintain at least a first order mismatch shaping functioning until the related SB comes out of its unstable situation [7]. On the other hand, Eq.3 is only applicable until the second layer. This is because the two first layers’ inputs can only lie between $[0,4]$ thus, Eq.3 recalls its origin from Eq.2. In conclusion, TDEM algorithm can hardly handle a pure simple second or higher order DEM. In [5], a mixed algorithm (MDEM) solved this problem by replacing a partially SDEM. It seemed to be a good idea but at the price of additional logic.

Recently, a hardware efficient STDEM solution was presented in [6] in which the first layer is completely eliminated, as shown in Fig.1.b. Here, the tree-structure DEM algorithm is well suited if there are no more than 4-DAC cells to control. Then, an ESB, which consists of three independent digital filters and one decision logic, controls each group of 4-DAC units (see Fig.3). Digital filters in the ESB can be a cascade of some (usually 2 or 3) integrators for lowpass and some resonators for bandpass applications. The decision logic is based on table-I, wherein the priority of any assignment for $S_{ij}$, $i,j \in \{1,2\}$ is forced to regulate critical volume in digital filters in the related ESB. Threshold levels $t_2$ and $t_1$ are depended on the filter’s order and structure which can be optimized by simulation or estimation. In order to fulfill number conservation rule and to be compatible with the rest of global TDEM, table-I must obey following expressions:

$$S_{11} = sv_1 - sv_2, \quad S_{21} = sv_1 + sv_2 - (sv_3 + sv_4)$$

$$S_{12} = sv_3 - sv_4, \quad y_{21} = sv_1 + sv_2 + sv_3 + sv_4 \quad (4)$$

Furthermore, to neutralize the input dependence at the following layers the special quantizer transfer functions of all the remained SBs are replaced by:

$$S_{kr}(n) = \begin{cases} +1 & y_{kr} \text{ odd and } V_{kr} > 0 \\ -1 & y_{kr} \text{ odd and } V_{kr} < 0 \\ +2 & 0 < y_{kr} < 2^k \text{ even and } V_{kr} > 0 \\ -2 & 0 < y_{kr} < 2^k \text{ even and } V_{kr} < 0 \\ 0 & \text{in all other cases} \end{cases}$$

(5)

By this mean, there is no serious instability problem in switching blocks any more since $S_{kr}(n)$ accepts a desired non-zero value for any non zero input to the related SB. The circumstances of this replacement were analyzed and a mathematical expression for a $b$-bit STDEM-DAC’s analog output $D_{OB}(n)$ is formulated in [6]. It is similar to that of TDEM in [4] as:

$$D_{OB}(n) = (1 + \overline{\epsilon})y_B(n) + e(n) + \epsilon$$

$$\overline{\epsilon} = \frac{1}{2B} \sum_{i=1}^{2^B} \alpha_i, \quad \epsilon = \sum_{i=1}^{2^B} \epsilon_i$$

$$e(n) = \sum_{k=1}^{B} \sum_{r=1}^{2^k-1} \Delta_{kr} S_{kr}(n)$$

$$\Delta_{kr} = \frac{1}{2k} \sum_{i=(r-1)2^k+1}^{(r-1)2^k+2^k-1} \alpha_i - \alpha_{i+2^k-1}$$

(6)

where $\overline{\epsilon}$ is a gain error and affects only the loop gain, $\epsilon$ is an offset error and $e(n)$ is an input depended nonlinearity error. The offset error $\epsilon$ cannot be corrected by DEM methods and normally does not have a destructive effect. The most important error is $e(n)$ which must be reduced towards zero in the band of interest. Regarding $e(n)$’s equation, all of the $S_{kr}(n)$ must be a vector with a desired shape through different digital filters. For example, a 3-bit feedback DAC mismatch-shaping system needs 7 digital filters feeding by 7 shaped-sequences $\{S_{31}, S_{21}, S_{11}, S_{12}, S_{21}, S_{11}, S_{12}\}$, in both TDEM and STDEM algorithms. However, in STDEM, these sequences can almost freely accept nonzero values even if they
receive even inputs. In fact, such a sequence has a much better match-shaping performance than that of a conventional TDEM, which is realized by merging two first layers and using dynamic decision rules in its true table as well as employing Eq.5 in the other layers.

III. CIRCUIT DESCRIPTION AND SIMULATION RESULTS

In today’s CMOS technologies, circuits’ mismatch standard deviation is in the order of a few tenths percents, (usually 0.1% < δI ≤ 1%). This level of mismatch causes noise floor and unwanted tones to be increased in the band of interest. Without any correction, the worst-case standard deviation of the normalized DAC-output for a B-bit thermometric structure can be expressed as [2]:

$$\delta [DAC_{out, dB}] = 20 \log \left( \frac{\delta I}{2^{2B} + 1} \right)$$

(7)

For example, suppose, δI = 0.01 and B = 3 results in a distortion of ≈ –70dB. In order to suppress this mismatch-noise in a high-resolution DSM (usually $DR \geq 90dB$), using a first order noise shaping is not sufficient. Thus, a 2nd-order lowpass or a 4th-order BP mismatch-shaping system will be needed regarding our applications1.

Fig.4 shows a modified switching-block diagram for a 4th-order BP-STDEM. It is completely realized in the digital domain. Since the output of the quantizer in a modified SB’s loop can accept a non-zero value for all of its non-zero inputs, the register’s resolution requirement is quite modest, maximum five-bit at last resonator ($V_{21}$).

Fig.5 shows the present design of the 4th order bandpass ESB wherein a sufficiently fluid group of decision rules is based on equations-4 and table-I. In order to estimate threshold levels $t_1$ and $t_2$, the critical volumes of digital filters’ output values have to be considered. For the loop containing $S_{21}, R_{21}$ and $V_{21}$, such a critical situation will start when the loop cannot be controlled for at least two periods ($S_{21} = 0$). If loop’s integrators (or resonators) have non-zero values just before receiving such a tail of zero $S_{21}$, the second integrator can be overflowed in some periods. For example, when integrators’ initial outputs are supposed to be 4 then, first one remainsunchanged but the second stage output (here $R_{12}$) becomes greater than 8 and $V_{21} ≥ 16$, while $S_{21}$ is still zero. Therefore, the threshold value $t_1$ has to detect such an output growing tendency. This can simply be realized by regarding present value of $V_{21}$ as in table-I. The estimated threshold level with this simple example is in the order of 16 and -16, respectively for positive and negative resonator’s output. However, we are naturally interested in its minimum possible value to strictly control registers’ values. Thus, in the same reasoning way but for one period of an unwanted output growing, a lowest threshold level estimated of about 8. In different practical simulations, these estimated values quietly results in proper mismatch shaping. The optimum value is obtained between 8 and 12, which is theoretically expected before. We can estimate the value of the second threshold level $t_{2, opt}$ in the same manner. The estimated $t_2$ value is 8. Its optimized value is 6. However, there is no much difference if it is practically considered $t_{2, opt} ≈ 8$. This method can also be used to estimate maximum resolution of the registers. If we suppose that such a critical situation can be present for about four further periods, the second register output ($R_{21, opt}$) can reach up to 28 which needs 5-bit resolution. This is well confirmed by different simulation, so that it rarely exceeds over 20. In order to give a better sense of this judgment, Fig.6 shows the registers’ output levels versus different DSM-input levels, where the same output of a conventional TDEM algorithm is depicted to be compared. Even-if one accepts using such a long register resolution, the mismatch-shaping action does

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1Note that a fourth-order bandpass noise-shaping centered at $f_s/4$ is equivalent to that of a similar second order lowpass one.
IV. CONCLUSION

A hardware efficient DEM algorithm and its related circuits were presented for a high performance multibit delta-sigma modulator. These circuits use an analytically discussed and optimized decision logic for a 4th order bandpass mismatch-shaping, which were also well confirmed by system and transistor level simulations. All advantages of a conventional TDEM algorithm are maintained while its instability disadvantage is eliminated by a dynamic sequence generation in modified structure. Designed circuits need a moderate area and can be clocked faster than a comparable algorithm such as SDEM.

REFERENCES