Frequency-Band-Decomposition converters using Continuous-Time Sigma-Delta A/D Modulators

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***Abstract*— Frequency-Band-Decomposition (FBD) is a good candidate to increase the bandwidths of ADC converters based on Sigma-Delta modulators, especially in the context of software radio, where very large bands need to be converted. Each modulator processes a part of the input signal band and is followed by an adapted digital filter. A new solution, called Extended Frequency-Band-Decomposition (EFBD) has been proposed during the ANR VersaNUM project, allowing large mismatches in the analog modulators without performance degradation, at the price of a calibration of the digital stage. This paper is an abstract of the whole project and presents its main results.**

I. Introduction

In the context of software radio, where very large bands need to be converted, the Frequency-Band-Decomposition (FBD) [1], [2] is a natural way to widen the bandwidth of Sigma-Delta converters [3], using parallel bandpass modulators. Each modulator processes a part of the input signal band [4]. Continuous-time (CT) modulators are the fastest technique as they possess one key advantage over their discrete-time competitors: no sampling is performed within the filter itself, allowing central frequencies in the gigahertz range. An implicit anti-aliasing is performed by the analog filter [5], thus reducing the constraints at the input of the converter.

The main issue of the FBD solution is its high sensitivity to the central frequencies of the bandpass modulators. Unfortunately, the filters of CT modulators are usually sensitive to process dispersion and temperature conditions.

Extended Frequency-Band-Decomposition (EFBD) [6] makes it possible to convert a wideband signal, using parallel continuous-time bandpass modulators. This solution is able to adapt to the analog mismatches of the modulators caused by variations in the manufacturing processes, in order to minimize the quantization noise of the system. As in many conversion systems, a calibration of the digital part of the EFBD becomes unavoidable.

This paper presents a full solution for an EFBD converter. The second section of this paper gives the global topology of the EFBD converter. The third section presents the design of the CT Sigma-Delta modulators. The fourth section presents the signal processing associated to the FBD converter. Finally, the fifth section concludes with the perspectives of this solution.

II. The Extended Frequency Band Decomposition solution

An EFBD is composed of $N+2$ parallel Sigma-Delta modulators (Fig. 1 - part A), where N is the number of modulators required to process the input signal band $[f_1 \dots f_2]$. Two extra modulators are used in the case of large analog mismatches so that the useful band $[f_1 \dots f_2]$ remains within the working band of the EFBD. The outputs of all channels are merged by a digital system (part B) to reconstruct the input signal.

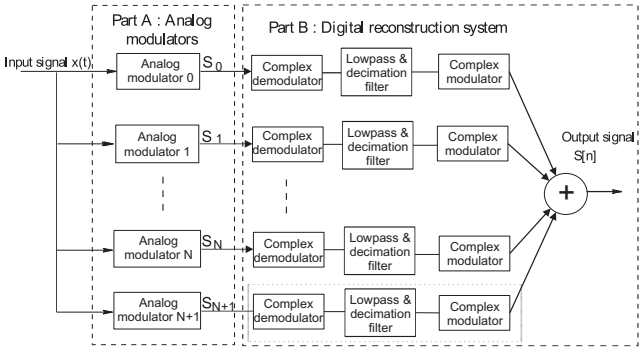

Fig. 1. Extended Frequency Band Decomposition architecture

Fig. 2 gives as an example, the noise power densities of each modulator (NTF^k), where all resonator frequencies differ from their ideal values by a constant value plus random mismatches (modelling process non-idealities). The Q factors of the filters are equal to 50. The boundaries between the band of each modulator are represented by vertical lines. In this example ($f_1 = 0.2, f_2 = 0.3$), the 10^{th} modulator is not used as its band is completely outside the signal band.

The benefit of the use of two extra modulators is shown in fig. 3, which shows the precision (in term of SNR) of an EFBD converter function of a shift of the central frequencies of all modulators. It was shown in [6] that after calibration, a shift of one subband on the left or the right does not have consequences on the performances of the converter.

III. CT modulators design

Our goal is to design wide-band Sigma-Delta modulators able to work with a central frequency between $0.2f_s$ and $0.3f_s$, where f_s is the sampling frequency. A sixth order topology has been chosen, which is a good compromise between performance, spurious-tones, stability and sensitivity to analog

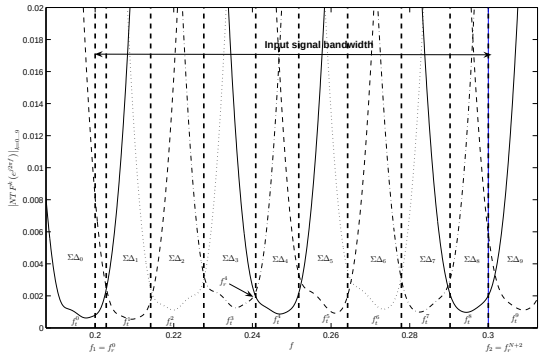

Fig. 2. Boundaries with non-ideal modulators

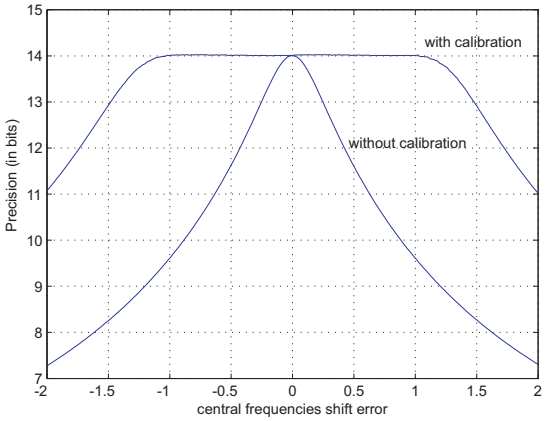

Fig. 3. Effect of a central frequencies shift on the performances of the bank

mismatches. The best way to design a CT Sigma-Delta modulator is to start from a discrete-time Sigma-Delta modulator filter transfer function, which satisfies all the demand in term of resolution and stability. Then, the transformation expressed in (1) will be used in order to achieve its CT Sigma-Delta filter counterpart.

$$F(z) = (1 - z^{-1}) Z_T\{L^{-1}[\frac{G(s)B(s)}{s}]\} - \underbrace{\sum_k a_k z^{-k}}_{D(z)} \quad (1)$$

L^{-1} denotes the inverse Laplace transform, Z_T the z-transform at sampling period T and $B(s)$ denotes the delay and non-ideality part of DAC and ADC functionality.

Among all the possible ways to realize the modulator's CT filters, we have chosen solid-state filters using lamb waves [7] [8]. The structure of Lamb Wave Resonator (LWR) which is similar to Surface Acoustic Wave resonator (SAW) and Film Bulk Acoustic Resonator (FBAR), is composed of a piezoelectric layer sandwiched between two thin electrodes and placed on a membrane. However, FBAR operates using vertical wave propagation; the LWR employs lateral wave propagation. Indeed, in LWR, the resonance appears when the length L is proportional to half wavelength. Changing the resonance frequency, while keeping standard lateral dimension, is possible through specific electrode designs [8]. The electrical model of a one-port LWR resonator is a RLC in parallel with a capacitor. The capacitor effect can be canceled using a differential amplification as shown in fig. 4 [9].

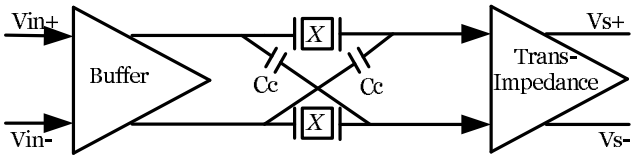

Fig. 4. Resonator topology

the resulting transfer function can be expressed as follow:

$$H_{res} = \frac{V_s}{V_{in}} = \frac{g_m C_m s}{1 + R_m C_m s + L_m C_m s^2} \quad (2)$$

The modulator topology must use filters with an enumerator containing only a term proportional to s. A candidate topology is given in fig. 5. The denominators of the filters ($dp1$ to $dp3$) have the same shape as (2). The NTF can be controlled by several degrees of freedom : coefficients $b'1, b'2, b'3, g1, g2, g3, g4, T2$, and the DAC delay. The optimal DAC delay will be equal to $1.95T_s$ for a central frequency equal to $0.2F_s$. It should be $1.08T_s$ for a central frequency equal to $0.3F_s$' [10].

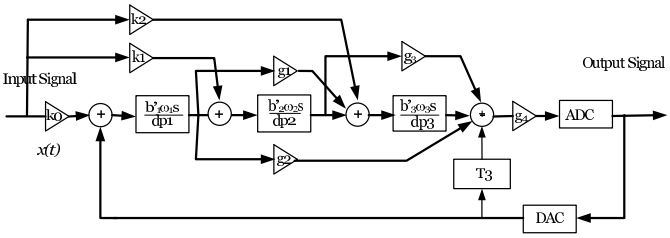

Fig. 5. Modulator topology

The signal transfer function will be controlled by coefficients k_0, k_1 and k_2. The whole analog filter realization, using differential elements is shown in fig. 6.

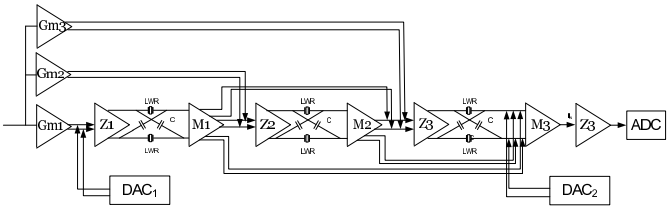

Fig. 6. Analog Filter

The Gm elements are voltage to differential current converters, the Z are dual current to voltage converters, and the M element are true differential current to current converters (current mirrors).

IV. Signal processing associated with a FBD converter

A. The digital processing of a FBD converter

The digital processing associated with each modulator is composed of a demodulation that brings the signal to baseband (demodulation frequencies are denoted f_C^k), of a comb filter that performs a decimation, of a FIR filter $H_k(z)$ that removes the out-of-band noise, of a signal transfer function correction $C_1(z)$ and of a modulation. The complete digital processing for one modulator is summarized in Fig. 7. The frequencies used for demodulation and modulation are expressed as rational numbers so that the sequences are finite and can be stored in a ROM [6].

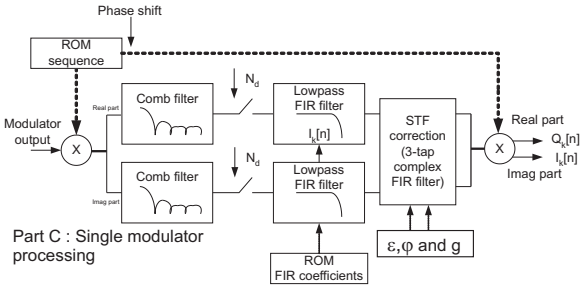

Fig. 7. Extended Frequency Band Decomposition architecture

The ROMs can possibly be replaced by spare logic if the ASIC technology does not allow user-defined ROMs. The computing resources needed for one modulator are summarized in table I. The first two columns of the table give the number of multipliers and adders required for each function. The two last columns give the synthesis results of each function in a $0.12\mu m$ digital technology in terms of flip flop number, gate number and area (mm^2). The synthesis has been performed from a VHDL model of each function. The target resolution is 14 bits. The FIR coefficients are quantized on 14 bits and the sine functions on 12 bits.

TABLE I

Computing resources for one modulator

	Multipliers	Adders ROM	FFD Gates	Area (mm^2)
Demodulation	0	$(N_{bit})*2$	140 2.5K	0.025
Comb filter	0 0	4*2 4*2	300*2 2.2K*2	0.025*2
Lowpass FIR filter	64*2	64*2	1.8K*2 15K*2	0.2*2
STF correction	8	10	630 6.8K	0.08
Modulation	4	2	140 2.5K	0.025

B. NTF Calibration algorithm

The NTF optimization of the system consists in using, for each frequency band, the modulator that has the best signal-to-noise ratio. As the signal transfer function is usually quite flat in the work band of the modulator, the modulator which is to be used for each frequency is the one whose noise power density is the lowest at this frequency.

The noise transfer function is optimized by tuning the boundaries between modulators $f_r^k, k = 1..N+1$ from f_r^{k-1} to f_r^{k+1}. The frequencies used for the modulator and demodulator are deduced from these values:

$$f_C^k = (f_r^{k-1} + f_r^k)/2, \tag{3}$$

and the bandwidths of the lowpass filters.

$$\Delta f_k = \frac{f_r^k - f_r^{k-1}}{2} \text{for } k = 1..N. \tag{4}$$

It has been shown in [6] that an error of 4% in the width of the subband (0.05% of the sampling frequency) causes a resolution loss less than 0.1 bit. Thus, the boundary frequency values (f_r^k) can be quantized with a step $q_s = F_s/1024$. The bandwidth of each subband would be 12 or 13 steps if all modulators were ideal.

The input of the EFBD must be first grounded. The noise power produced by the quantization is minimized by varying the values of the boundary frequencies f_r^k. The demodulation sequence and the lowpass FIR filters are fully determined by the knowledge of these values ((3) and (4)).

The adaptation scheme given in Fig. 8 was used. The scheme itself uses the processing of the digital part presented in Fig. 7. The estimate of the converter noise power is:

$$\hat{P} = \frac{1}{N_s} \sum_{n=1}^{N_s} \sum_{k=1}^{N+2} (I_k[n]^2 + Q_k[n]^2) \tag{5}$$

N_s is the number of samples used for the power estimation, I and Q are the outputs of each filter (Fig. 7) .

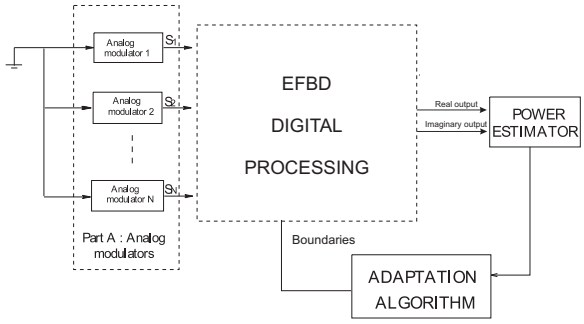

Fig. 8. Quantization noise minimization

The proposed algorithm is based on a so-called relaxation method. Initial values are those obtained theoretically (i.e. design typical values). The algorithm changes iteratively the boundary value f_r^k between f_r^{k-1} and f_r^{k+1} for $k = 1$ to $N+1$ in each sequence. The first boundary remains f_1 and the last boundary remains f_2.

This algorithm has also been tested in a simulation. The result is given in Fig. 9. We verified that the convergence to the optimum value is also reached after three sequences for

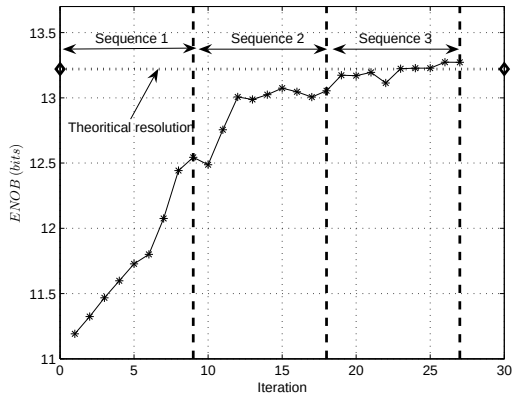

Fig. 9. Evolution of noise power during iterations -on line-

all kind of mismatches (with systematic or random errors on the modulator's central frequencies).

With 400 MHz analog frequency, each noise power calculation performed from 4000 samples takes 10 μs to perform (the OSR of the system is equal to 5), and each sequence in the worst case approximately 2.25 ms (9 boundaries are varied among 25 values). The total NTF calibration time for 3 sequences can be estimated to 6.8 ms.

C. STF calibration algorithm

The proposed optimization algorithm (Fig. 10) uses as input a one-bit signal generated by a Sigma-Delta generator such as the one proposed in [11]. The analog continuous-time modulators and the FIR filters sufficiently filter the signal so that the quantization noise power becomes negligible in front of the input signal power.

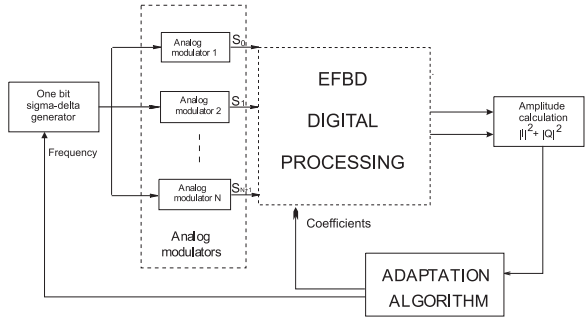

Fig. 10. STF flattening

If the system was perfect, the output signal power would be constant when the input frequency varies. Unfortunately, the modulator transfer functions are not flat. They can be calculated by methods proposed in [12] and, usually, the modulus of the STF can be approximated by a parabola whose maximum is in the band of the modulator [6]. A corrective filter is here applied to each modulator to flatten its signal transfer function.

Furthermore, there is a phase shift between adjacent modulators. This phase shift is corrected by changing the phase of the modulation sequence used in the last stage of the digital processing [6].

The STF calibration is performed in two steps: first adjust the transfer function of each modulator, then adjust the phases between adjacent stages. The whole algorithm is presented in [13]

V. Conclusion

This paper described the design of a whole frequency-band-decomposition converter composed with bandpass Sigma-Delta modulators. A topology for sixth-order bandpass continuous-time Sigma-Delta modulators was proposed. this topology permits the design of modulators with a wide range of central frequencies. This topology is adapted to a large kind of bandpass filters (LC filters, SAW, BAW, LWR filters). The digital processing associated to this filter bank has also been completely defined as well as the calibration algorithms in order to become immune to most of analog mismatches. The whole calibration process proposed in this paper can be performed in few ms, which is compatible with the power-up time of any communication system. All this study concludes positively about the possibility to build wideband converters using parallel Sigma-Delta modulators without requiring a strict analog trimming.

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