A clock network of distributed ADPLLs using an asymmetric comparison strategy

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***Abstract* — in this paper, we describe an architecture of a distributed ADPLL (All Digitall Phase Lock Loop) network based on bang-bang phase detectors that are interconnected asymmetrically. It allows an automatic selection between two operating modes (uni- and bidirectional) to avoid mode-locking phenomenon, to accelerate the network convergence and to improve the robustness to possible network failures in comparison to simple unidirectional mode.**

I. INTRODUCTION

Balanced clock trees used in most modern synchronous digital integrated circuits and microprocessor systems [1] suffer from two main drawbacks. The first one is the phase difference (called the skew) of the distributed clocks and the second one is the extra-power consumption mostly due to thermal losses. Both of these limiting factors are generally related with inter-lines coupling, important parasitic impedances and random parametric variation of the clock buffers [2]. Moreover, these problems become more critical as frequency increases, thus they have a major impact on the overall system design and performance.

An interesting alternative to conventional balanced trees is an active clock distribution network using at each node a local Phase Locked Loop (PLL) to ensure synchronization [3, 4]. The idea is to use equidistant clocks on the chip and to ensure their synchronization by adjusting their phase according to that of the clocks in the immediate neighborhood. This architecture only requires local synchronization between adjacent nodes to produce a global synchronous clock. Moreover, since wires are only used to interconnect neighboring nodes, they can be short and narrow: this reduces the parasitic capacitances and hence, the power consumption and the random skew.

However, due to the cyclic nature of the phase, a distributed PLL network may stabilize under a parasitic working mode called "mode-locking" where constant non-zero phase differences can exist between PLL oscillators. This unwanted regime can be suppressed using some specific phase detectors that have a negative slope beyond a phase difference of $\pi/2$ [3, 4]. Unfortunately, the practical implementation of these phase detectors is not trivial [4]. In our previous work [5], we have proposed another mode-locking cancellation solution consisting in ensuring that no feedback loop exists in the propagation of the phase information (unidirectional mode). This approach presents two main drawbacks, the convergence time of the network and the system robustness to network failures. Important convergence time is mainly due to the fact that the phase propagation is done in one direction restricting feed-back information. Although convergence time is not critical while the system starts up, it is much more an issue for stability reasons in the steady state regime while the system is stressed under external perturbations. Moreover, unidirectional approach increases the risk of overall system dysfunction due to possible nodes failures like for example in the case of a chain with a broken link.

In this paper, we propose a simple strategy allowing automatic selection between a network with and without feedback loops (bi- and unidirectional modes) in presence of mode-locking threat. This solves the mode-locking problem and, in the same time, gets less critical the drawbacks mentioned above.

In section II, more details on the active clock distribution network and the mode-locking phenomenon are illustrated. Then in section III, the switching strategy and in section IV, some comparative simulation results are shown. Finally to conclude, some perspectives are given to this work.

II. ACTIVE CLOCK DISTRIBUTION NETWORK

The active clock distribution network and its synchronization mechanism are illustrated in Figure 1. The architecture is composed of independent oscillators that are separated spatially (in the present case, digital controlled oscillators (DCO) represented with blue circles in Figure 1) connected in a two dimensional regular grid with phase detectors (PD, represented with black rectangles in Figure 1) and filters (for clarity reasons, not represented in Figure 1). The PDs[1], filter, DCO and its interconnections constitute a node of the phase locked loop (PLL) network with multiple input signals. Each phase detector is located right in between two adjacent oscillators so that it mutually compensates the clock propagation delays from one oscillator to another one.

[1]The number of PDs (2 , 3 or 4) depends on the DCO position in the network

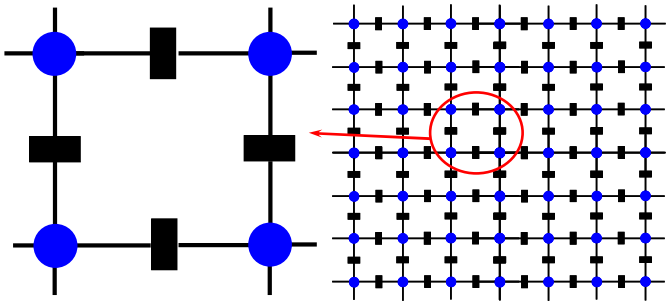

Figure 1. Active clock distribution network

The global synchronization is achieved in the following way: the DCOs generate independent clocks distributed through the chip; the PDs of each node detect the phase differences between adjacent clocks and the output of the node's local oscillators; the averaged total errors finally are used by the filters to adjust the local clock frequencies. After a transient period, the local clocks are synchronized with the average clock signal delivered from their neighbors. If it is the case for all PLLs in the system, then the overall network should be globally synchronized.

However, synchronization in phase is not always achieved. Indeed, a situation where all the nodes are synchronized only in frequency and not in phase with their neighboring nodes can exist. That is due to the cyclic nature of the phase. This undesired mode, known as mode-locking [3, 4], can be observed in the example of a 2x2 network presented in Figure 2.

As the phase is cyclic ($-\pi/2=3\pi/2=7\pi/2$), in this particular configuration, phase differences between neighboring nodes and the local clock exactly compensate themselves. Since the phase error at every node is zero, there is no reason for the phase to change and the network stays in this stable parasitic stationary point.

The mechanical representation of this phenomenon is illustrated in Figure 3. Here, oscillators are represented by sustained masses (blue circles), their phases by corresponding angular position and their interconnections by springs. In this particular position all restoring forces are mutually compensated and system stays in this parasitic stable configuration.

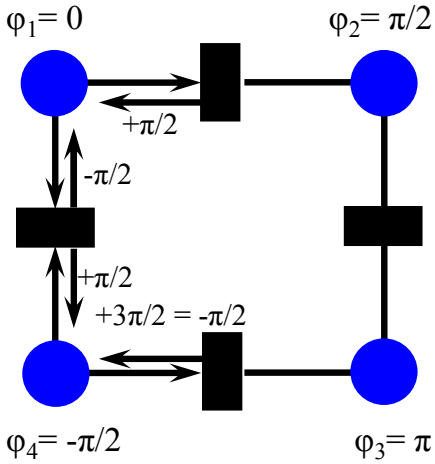

Figure 2. Mode-locking example in a 2x2 network

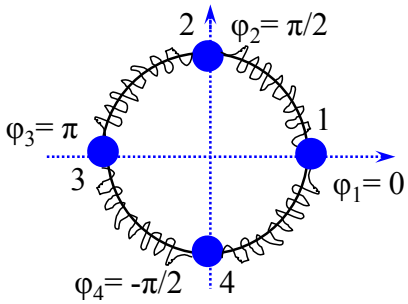

Figure 3. Mechanical representation of mode-locking phenomenon

To avoid this phenomenon, in previous work [5], we have adopted a unidirectional information propagation of the phase. It is equivalent in the mechanical representation of the system to break one of the springs. In the next section of this paper, we go one step further by introducing a mixed architecture that allows uni- and bidirectional phase information propagation.

III. SWITCHING STRATEGY

The proposed "switching strategy" consists in adapting dynamically the architecture between bidirectional and unidirectional modes when mode-locking risk is detected. It is based on an "all digital" PLL (ADPLL) network architecture, and in this context can easily be implemented.

A. ADPLL description

Figure 4 presents the all digital PLL with multiple inputs as a node of the considered network. Depending on its position in the network, the ADPLL has two (corner), three (side) or four (inside) inputs. The so-called bang-bang phase detectors (BB-PD) used in this architecture have a 1 bit output that detects if the reference clock (from neighboring clocks) is in advance compared to the local clock or not. In the phase domain, BB-PDs are modeled with the sign function as shown in Figure 5. If the phase error is positive i.e. the reference signal comes earlier than the local signal, the phase detector output is +1 otherwise it is -1.

Finally, outputs of all BB-PDs are summed and filtered by a digital PI filter (F) in order to adjust the local DCO frequency. Please note that BB-PD exhibits an infinite dynamic range in terms of phase difference and can therefore be used as well as frequency detector (PFD). As a conesquence, that kind of ADPLL with BB-PD has an infinite locking region. For more details on BB-PD, readers are invited to refer to [6].

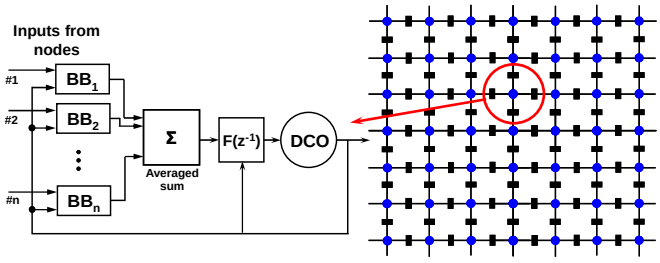

Figure 4. The proposed ADPLL network. DCO stands for Digital-Controled oscilaltor, F the filter, BB the bang-bang phase detector.

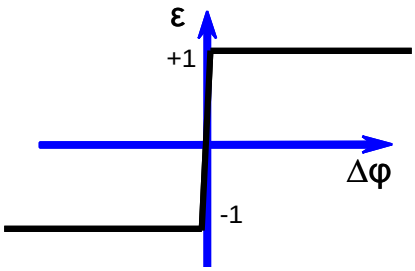

Figure 5. Bang-bang phase detector static response in phase domain

B. *Mode-locking risk suppression*

To eliminate mode-locking failures, some directions of the phase propagation are weighted using appropriate coefficients in the error sum of the BB-PD outputs. In a sense, a kind of asymmetry is introduced in the comparison strategy of the network. Since the output of BB-PD is one bit, it may completely inhibit some directions of the phase information propagation (realizing a unidirectional mode) only if the node is mode-locked. Otherwise, if the node is far from mode-lock mode, it uses the information coming from all directions to ensure bidirectional synchronization.

Let us demonstrate this automatic mode-locking rejection in the example of a 2x2 ADPLL network (Figure 2). In this example, all of the nodes have an identical frequency and 2 inputs coming from neighboring nodes. For sake of simplicity and since each nodes have the same working conditions, we take into account only the first node associated with its local clock and consider its two neighboring clocks as references with constant frequencies (named ref_1 and ref_2 in figures 6 and 7). In the traditional active network without an asymmetric comparison strategy and considering the initial conditions represented in Figure 6, the node dynamic has the following behavior. First stage, the network is not mode-locked; the local phase (red line) is in advance compared to the reference phases (ref_1 and ref_2, blue lines), so both PDs give error "-1"; total error is "-2" and the local phase is decreasing. Second stage, the local phase is bounded by the two references; first PD output is equal to "+1" while the second one is "-1"; the total error is zero, so the local phase continues to grow with a constant central oscillator frequency (inclined red line in Figure 6). Note that such parasitic compensation can be achieved in the same time for all nodes of the network (Figure 2) and mode-locking regime can subsist for a long time.

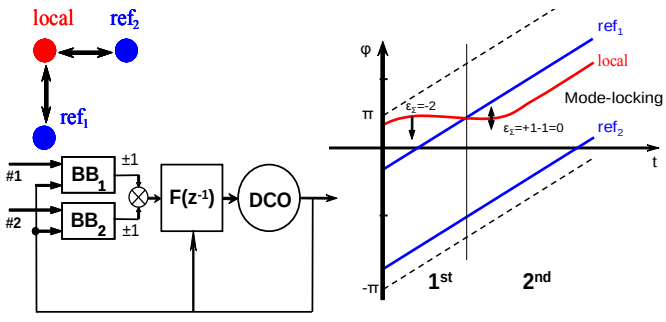

Figure 6. Node without assymetric comparison strategy, mode-locking

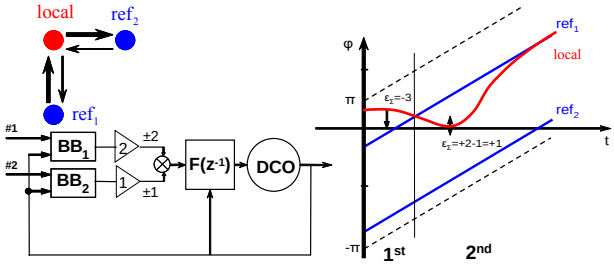

Figure 7. Node with assymetric comparison strategy, mode-locking avoidance

In the proposed asymmetric comparison approach using weighting coefficients in the error sum, the node dynamic has the following behavior (Figure 7). First stage, BB_1-PD gives an error of "-1" multiplied by coefficient 2, and BB_2-PD output is "-1" multiplied by 1; the total error signal is equal to "-3" and the local phase is decreasing taking into account both references. In the second stage, when the local phase (red line) is in the bounded area (between ref_1 and ref_2, blue lines), BB_1-PD output is "+2" while BB_2-PD output is "-1"; because of the bang-bang PD characteristic (1 bit quantization of the error signal), BB_2-PD output signal is totally compensated by BB_1-PD output signal; the remaining error is therefore equal to "+1" and the local phase is forced to be equal to the first reference (ref_1) ignoring the second one. In this particular regime, the local node ignores the ref_2 clock signal and tracks only the ref_1 clock signal like for a one input PLL. This situation corresponds to a unidirectional mode of the phase information propagation ensuring the mode-locking regime suppression [5].

The main advantages of the proposed architecture are the following. The bidirectional and unidirectional mode selection is made automatically in presence of a mode-locking threat. Moreover, since this architecture uses all phase information when the network is far from the mode-locking, it guarantees a fast convergence and robustness of the network.

IV. SIMULATION RESULTS

Simulations of a 2x2 ADPLL network with and without the asymmetric comparison strategy were performed in order to compare results between the two networks. In both cases, initial conditions are the same: node 1 is the master clock, it is considered as the reference clock signal with a constant radial frequency (2π rad/sec) and a zero initial phase. Note that these simulations have been done with an arbitrary central frequency because the existence of mode-locking regime is only dependant on the network topology.

From Figure 8, one can see that the network with the symmetric comparison strategy reaches synchronization in frequency but not in phase although the total error in phase is null. The network is therefore in a stable mode-locking regime that cannot be suppressed. On the contrary, the network with the asymmetric comparison strategy synchronizes in frequency and phase without any mode-locks as illustrated on figure 9. Residual oscillations on the frequency error are due to the nature of bang-bang phase detectors as for sigma-delta converters. Simulations on a 4x4 ADPLL network have shown similar results.

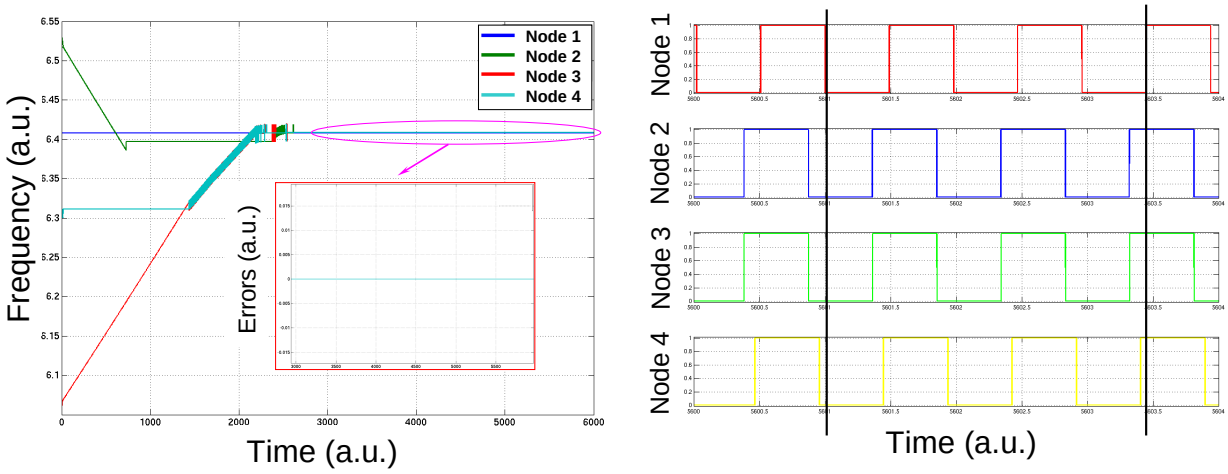

Figure 8. Simulation results on a 2x2 network with a symetric comparison strategy: frequency of the nodes and a zoom on their errors with the master clock (left), temporel signal in steady state of each generated clock (right)

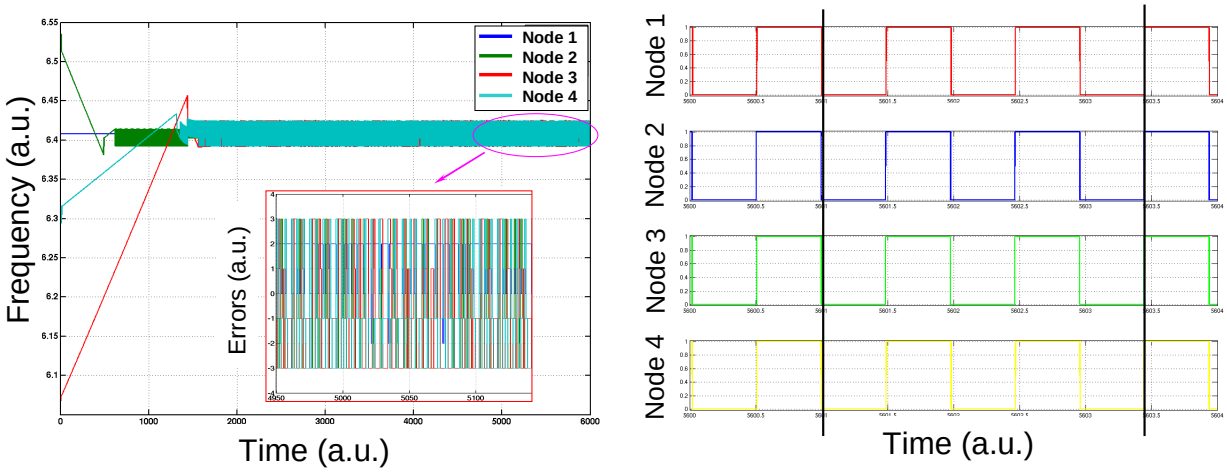

Figure 9. Simulation results on a 2x2 network with an asymmetric comparison strategy: frequency of the nodes and a zoom on their errors with the master clock (left), temporel signal in steady state of each generated clock (right)

V. CONCLUSION

An active clock distributed network and its synchronization with locally generated independent clocks was described in this paper. Because of mode-locking risk in this kind of structure, it requires special attention in the phase information propagation inside the network. This work has demonstrated a novel asymmetric phase comparison strategy allowing automatic bidirectional to unidirectional selection of the phase information propagation while the system enters in a mode-locking regime threat. Simulations have been performed to illustrate the efficiency of the approach. We are actually working on the design of an optimal PI controller in order to minimize residual oscillations on the DCO command signal and to guaranty as well acceptable convergence time of the network. A physical implementation of such a network is on its way on a 65nm CMOS technology.

ACKNOWLEDGEMENTS

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