Wide-band multipath A to D converter for Cognitive Radio applications

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***Abstract* — This article presents a digital-enhanced radio frequency receiver for fast wide-band spectrum sensing. It is based on charge sampling and hybrid filter bank techniques. The charge sampling method is employed to design analog bandpass filters. Using a hybrid filter bank for wide-band analog-to-digital conversion improves the speed and resolution of the conversion. We propose to use these techniques in combination of frequency-division multiplexing with time-division multiplexing to design an integrated, completely software reconfigurable and reliable back-end of radio frequency receiver for cognitive radio applications.**

***Index Terms* — Analog-digital conversion, ADC, Bandpass charge sampling, Integration sampler, Hybrid filter bank, Wide-band receiver, Wide-band sensing.**

I. Introduction

The term of "Cognitive Radio" was coined by Joseph Mitola in 1999. It describes a radio where hardware parameters are defined by software. Furthermore such a radio link is aware of its surrounding and adapts intelligently. Future wireless communications systems should benefit from the cognitive radio approach to achieve high data rate services while managing interferences. Cognitive radio is indeed an emerging concept in wireless access, aimed at vastly improving the radio spectrum use by reusing unoccupied spectrum "holes" while minimizing the generated interference. The principle of cognitive radio is to detect transmission opportunities in spatial, temporal and spectral domains and reuse them to deploy new opportunistic services without causing any harmful degradation to the other systems in the band.

Spectrum sensing function (SSF) is arguably the most important task for the establishment of cognitive radio. SSF includes awareness of interferences and presence of primary users.

This work is part of a project studying cognitive radio systems to fulfill the needs for seamless mobile connectivity and optimum spectrum management. This paper focuses on the radio frequency (RF) receiver, especially on the sampling and quantization process for wide-band and reliable spectrum sensing. SSF can be realized in two steps:

- *Wide sensing:* coarse exploration of the whole band to discriminate used and available frequency bands;
- *Fine sensing:* focusing on some bands selected trough wide sensing with a higher resolution to find more information about them, their occupation and availability.

The requirements for this receiver are wideband conversion, software reconfigurability, CMOS integrability.

This paper is organized as follows. Section II introduces the hybrid filter bank (HFB) architecture for wide bandpass analog-to-digital conversion (ADC). Section III presents the bandpass charge sampling (BCS) technique and its use in a HFB context. Section IV presents the studied system specifications. Simulation results are shown in Section V.

II. Hybrid Filter Bank Analog to Digital Conversion

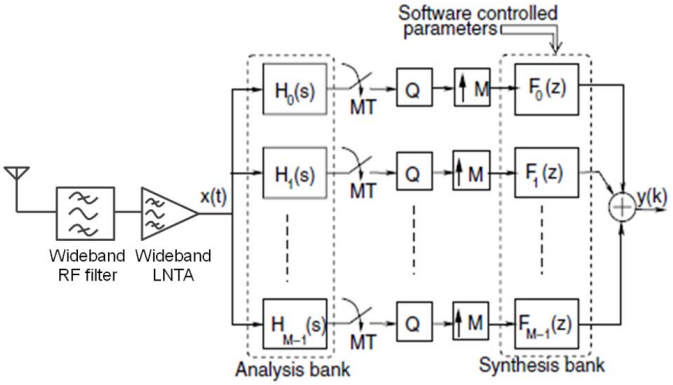

Fig. 1. Front end with Hybrid Filter Bank ADC.

The proposed RF receiver architecture is shown in Fig.1. RF filters limit the reconfigurability of the receivers and current research works toward the suppression of these filters (SAW-less architecture). In this work, it is however decided that at the beginning of the project, the RF filter is still used in order to relax the requirement on both the low noise amplifier and the back-end stage. After the wideband RF filter, a wideband (or multi) low noise transconductance amplifier (LNTA) is used, which allows to implement bandpass charge sampling filters (see section III). The RF signal is then processed by a parallel M-path HFB by employing bandpass charge sampling filters as analysis filters ($H_i(s)$ in Fig. 1). On each path the subband signals are sampled at $F_s = F_{OUT} / M$, where $F_{OUT} = 1/T$ is the effective sample rate of the system, and converted to digital signals with a n-bit quantizer. The resulting digital signals are then upsampled by M and filtered by the digital "synthesis" filters $F_i(z)$. The effective sample rate of the system is M times that of the subband quantizers. In this hybrid filter bank (HFB) architecture, the digital synthesis

filters are computed to minimize reconstruction error (see section V).

Another interesting feature of HFB is the frequency focusing (FF) capability [2]. The digital synthesis filters coefficients can be computed to get a constant resolution over the whole band, or rather achieve a higher resolution on a selected narrower band.

In most HFB architectures, analog filters are continuous-time. Continuous-time filters are well suited for very high speed applications and can offer high signal-to-noise ratio (SNR). However HFB architecture is highly sensitive to analog imperfections, and manufacturing errors of continuous-time filters that become more and more inaccurate in advanced CMOS technology. Furthermore, the architecture of a continuous-time filter becomes increasingly complex and expensive to integrate as the filter order or the quality factor becomes higher [3]. That is why we propose to use bandpass charge sampling filters as analysis filters.

III. Bandpass Charge Sampling

The bandpass charge sampling (BCS) filter [4] (also called bandpass integration sampler [5]) provides the above-mentioned requirements for the design of a digital enhanced receiver: BCS are simple (only switches and capacitors), CMOS integrable [6], and robust to nonidealities such as clock jitter [5]). The input waveform is integrated over a fixed time window, and the resulting integral is taken as a sample. The window can approach the sample period, and its repetition rate defines the sampling frequency. Fig. 2.a shows the bandpass charge sampling (BCS) filter architecture, and Fig.2.b shows its clocks scheme.

The first element, the transconductance G_m, represents the last stage of the LNTA. Its output i_{in} is a differential analog current signal. During the integration window T_i the switches are turned on alternatively at frequency F_c. The resulting chopped current is integrated into the capacitor C_s. At the end of the integration window the sampled voltage on the capacitor is read in V_{out} through charge transfer during the time Δs. Then the capacitor is reset during the time Δr.

Thus, the BCS combines a filtering and a sampling function. The filtering transfer function is a cardinal sine centered on frequency F_c and with notches located at $F_c \pm k.F_i$ for all k in $\mathbf{Z}^*$[6]. Fig. 3 shows this transfer function for F_c=900MHz and two values of F_i. This filtered signal is sampled at frequency F_s.

T_i is limited by T_s and technology speeds since $T_s = \Delta r + T_i + \Delta s$. Thus with this architecture F_i will always be higher than F_s.

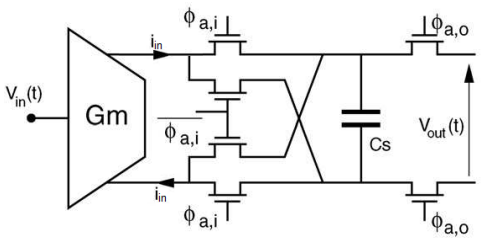

Fig.2.a Bandpass Charge Sampling architecture.

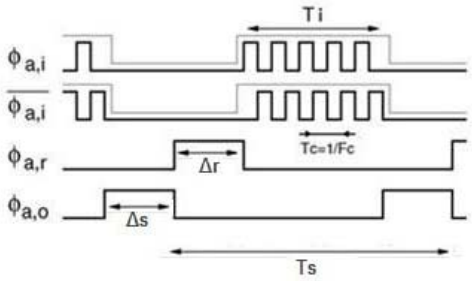

Fig.2.b BCS clock scheme.

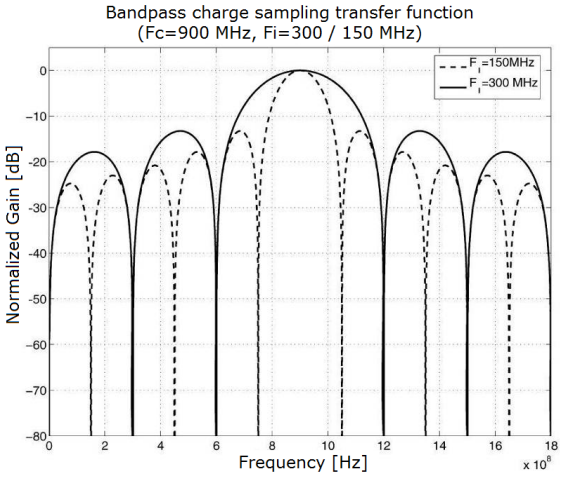

Fig.3. Example of frequency response of a BCS filter.

IV. System Specifications

The HFB architecture proposed in this paper includes BCS filters as analysis filters. Considering the properties of the BCS filters seen above, parameters F_c and F_i of each filter can be chosen to maximize the performance of the system, F_s being fixed at $2*B/M$ (see section II).

The rest of the paper examines the variations of the performances of the system with respect to these parameters under some chosen specifications. These settings are:

- The frequency band of the input signal is [954-1762] MHz, corresponding to a bandwidth of 808 MHz.
- The total band converted by the quantizers, which must be slightly wider than the input band to ensure acceptable performances for any HFB, is [900-1800] MHz.

- This band is divided into M=8 sub-bands, each being processed by a single quantizer. The sampling frequency is then F_s=225 MHz.

With these settings, there are 16 parameters to tune, two for each BCS filter. To reduce this number, we made the choice to fix the central frequency of each BCS filter on the medium frequency of its sub-band, which seems like a reasonable choice. The value of parameter F_i was also chosen to be the same for all filters.

It seems likely that the results in section V can be partially generalized to any specification.

The performance of the architecture is measured by the Signal-to-Noise Ratio (SNR) defined for an input frequency f as:

$$\mathrm{SNR}(f) = 10\log_{10}\frac{\left|\mathrm{Trans}(f)\right|^2}{\sum_j \left|\mathrm{Alias}_j(f)\right|^2 + psde.\sum_{k=1}^{M}\left|F_k(f)\right|^2} \qquad (1)$$

where Trans(f) is the transmittance introduced by analysis and synthesis filters, Alias$_j$(f) is the j-th aliasing term produced by sub-sampling, *psde* is the power spectral density of quantification error (considered here as a white noise so *psde* is constant over the frequency band), and F_k is the transfer function of synthesis filter k.

In the same way the overall performance is defined as the global SNR over the whole frequency band:

$$\mathrm{SNR}_{\mathrm{tot}} = 10\log_{10}\frac{\int_B \left|\mathrm{Trans}(f)\right|^2.df}{\int_B \sum_j \left|\mathrm{Alias}_j(f)\right|^2.df + \int_B psde.\sum_{k=1}^{M}\left|F_k(f)\right|^2.df} \qquad (2)$$

This measure is related to the global resolution of the wideband ADC since 6dB of SNR correspond roughly to a resolution of 1 bit.

V. Results

For a given set of analysis filters, the Least Mean Squares Global Approximation method [2] computes the digital filter bank that minimizes the reconstruction error on the band (which takes into account the distortion, aliasing and quantification noise effects). This reconstruction error can be weighted to maximize the resolution over a selected narrower band, allowing for the frequency focusing feature.

Due to the specificity of BCS filters, the performance of the resulting HFB can be improved by introducing phase diversity between the paths of the HFB. Consequently small delays are added between the sampling instant of BCSs. We define δ as the delay between the sampling instant of two consecutive BCS (so if the first BCS samples at instant nT_s, the i-th BCS samples at instant $nTs + (i-1).\delta$). This modifies the phase of the transfer function of each BCS filter and leads the architecture to be a combination of frequency-division multiplexing with time-divison multiplexing. To help the comparison with time-interleaved architectures, we introduce the normalized delay

$$d = \delta.\left(\frac{T_s}{M}\right)^{-1} \qquad (3)$$

T_s/M being the delay introduced between paths in a time-interleaved architecture.

Similarly, to ease the generalization of the results, a normalized width parameter is defined as

$$r = \frac{2*T_s}{T_i} = \frac{F_i}{B/M} \qquad (4)$$

Given the condition $F_i > F_s$, the value of r must be greater than 2.

The overall performance of the system is limited by the resolution of the quantizers and the number of coefficients of the FIR synthesis filters. Figures 4 (resp. 5) shows the variation of this performance with respect to d (resp. r) for various values of r (resp. d), when the quantizers have a resolution of n=14 bits (corresponding to a maximum SNR$_{\mathrm{tot}}$ of 86dB) and the analysis filters have 128 coefficients.

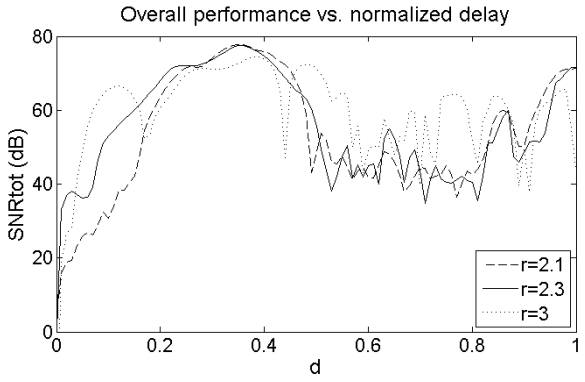

Fig.4. SNR$_{\mathrm{tot}}$ versus normalized delay d for various values of r.

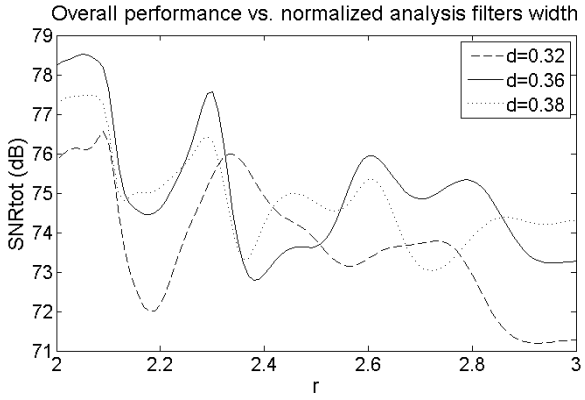

Fig.5. SNR$_{\mathrm{tot}}$ versus normalized delay r for various values of d.

As can be seen on Fig. 4, the conditioning problem induces poor performances when d is near 0, but the resolution approaches the ideal value (n=14 bits) for values of d between 0.25 and 0.4. For those values, the performance does not vary much with respect to r, but is rather better for low values of r. However very low values could be difficult to implement in practice due to technological minimum for Δr the capacitor reset time and for Δs the sampled charge transfer time. Considering this, d=0.36 and r=2.3 could be reasonable and near optimal values for the parameters.

With these specific values, the global SNR is 77.4dB, which corresponds to about 13 bits of resolution. Figure 6 shows the SNR versus frequency in this case. It can be noted that the SNR is almost constant on the whole band, except near the borders of the band, where it decreases somewhat substantially. This could be improved easily by slightly increasing the sampling frequency of the quantizers and is the subject of further work.

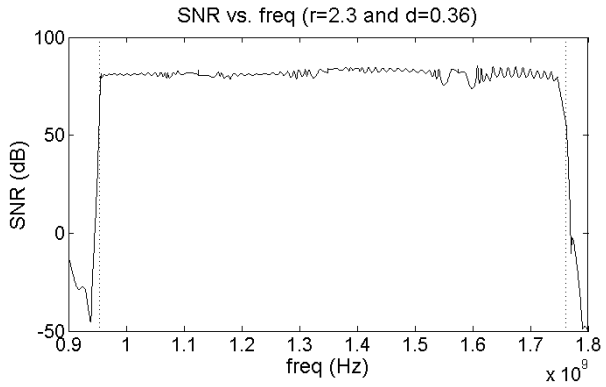

Fig.6. SNR versus frequency for near optimal values of the parameters (r= 2.3 and d=0.36) and 128-tap synthesis filters.

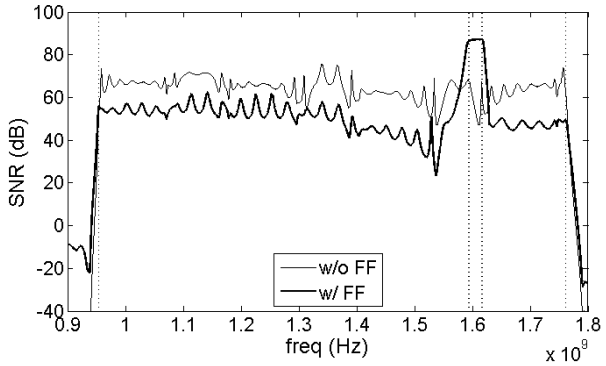

Fig.7. Illustration of the frequency focusing feature: SNR(f) of the system with 64-tap synthesis filters without and with frequency focusing over a 24MHz band around 1.6GHz.

The overall performance of the ADC being near the maximum obtainable performance (86dB) given the resolution of the quantizers, the frequency focusing feature cannot improve it much on a narrower selected band. The interest of this feature can yet be illustrated when the number of coefficients of the FIR synthesis filters is reduced, which diminishes the overall performance of the ADC. To this aim, Fig. 7 compares the SNR versus frequency with and without frequency focusing, when the number of coefficients is 64 instead of 128.

VI. Conclusion

Combining bandpass charge sampling filters with hybrid filter banks offers a promising and potential solution for designing wideband A to D conversion in the context of a digital-enhanced radio frequency application. The proposed resulting architecture is a combination of frequency-division and time-division multiplexing.

Optimizing the BCS filters parameters, we showed that this architecture is very suitable for spectrum sensing feature: It can approach the ADCs resolution over a wide band, provided that the digital complexity is sufficient; or with lower digital complexity the frequency focusing feature can improve resolution on any shorter frequency range.

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