A Design Approach for Networks of Self-Sampled All-Digital Phase-Locked Loops

Jean-Michel Akré, Jérôme Juillard, Mohammad Javidan, Eldar Zianbetov, Dimitri Galayko, Anton Korniienko, Eric Colinet

A Design Approach for Networks of Self-Sampled All-Digital Phase-Locked Loops

J.M. Akre and J. Juillard
SUPELEC
Plateau de moulon, France
Email: jean-michel.akre@supelec.fr

M. Javidan, E. Zianbetov and D. Galayko
LIP6 - UPMCE
4, Place jussieu, Paris, France
Email: mohammad.javidan@lip6.fr

A. Korniienko and E. Colinet
CEA-LETI, MINATEC
17, rue des martyrs, Grenoble, France
Email: anton.korniienko@cea.fr

***Abstract*—This paper addresses the problem of the stability and the performance analysis of N-nodes Cartesian networks of self-sampled all digital phase-locked loops. It can be demonstrated that under certain conditions (such as filter coefficients value) a global and a local synchronization can be obtained. Our approach to find the optimal conditions consists in analyzing an corresponding linear average system of the Cartesian network rather than constructing a piecewise-linear system which is extremely difficult to analysis. The constructed corresponding system takes into account the non-linearity of the network and especially the self-sampling property. It is then analyzed by linear performance criteria such as modulus margin to guarantee a robust stability of the Cartesian network. The reliability of our approach is proved by transient simulations in networks of different sizes.**

I. Introduction

The problem of clock distribution in complex high-frequency synchronous digital circuits such as synchronous Multi-Processors Systems On Chips (MPSOCs) is widely investigated in numerous studies [1], [2], [3], [4]. Centralized clock distribution technique (clock trees and grids) are no more suitable for such a systems: despite the need to do so, it is difficult to distribute a low skew clock over a wide geographical area. To improve the precision of centralized clock distribution, local dynamic correction methods based on programmable delays, buffers, etc are necessary which increase significantly the power consumption and the area of the chip [1], [5].

An alternative to solve the problem of scalability and skew is decentralized clock distribution technique based on mutually synchronized oscillators networks. The oscillators are distributed over the chip area. Each oscillator is coupled with its neighbors to guarantee the synchronization between all neighboring synchronous areas and by the same way the synchronization of the entire system. The feasibility of decentralized clock distribution networks has been proved originally by Pratt and Nguyen in 1995 [1] and afterward by other works [2], [3], [4]. Most of these works rely on techniques of analog circuitry which are hard to integrate in digital chips. According to our previous works [6], [7] this drawback can be overcome by considering a network composed of N-nodes of identical Self-Sampled All-Digital Phase-Locked Loops (SS-ADPLLs). A typical SS-ADPLL can be broken down into three blocks (Fig. 1): Phase-Frequency Detectors (PFD) which produces information about the phase differences between the local and the neighbors clock signal, a discrete filter which processes the sum of the PFDs output and commands the oscillator. The third block is a Digitally-Controlled Oscillator (DCO) which produces the local clock signal.

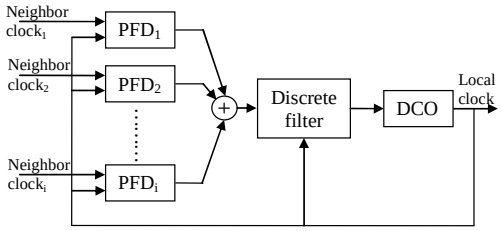

Fig. 1. Architecture of a typical SS-ADPLL.

Because of the self-sampling property and the existence of PFDs in the loop, an ADPLL is a strongly non-linear system. The study of the stability of a network of SS-ADPLLs can be broken down to the study of the stability of a Piecewise-Linear System (PLS), parameterized by the coefficients of the loop filter and the number of nodes in each line and column of the network. In this approach, some quantitative measures of stability and performance (settling time) are characterized by using Lyapunov functions or storage functions. Then the design parameters are incorporated into an optimization problem to optimize these quantitative measures for the closed loop system. This approach presents extreme numerical difficulties with solution time exponentially arising in function of the network dimension i.e NP-hard problem. In this work it is shown that for some particular network architectures (such as Cartesian networks) of SS-ADPLLs, the stability and the performance analysis can rely on the analysis of its corresponding linear average system. The main contributions of this work are: 1- the construction of the corresponding average system of a N-nodes Cartesian network and 2- the calculation of the optimal filter coefficients to guarantee the stability and the performance (settling time) via a linear performance criterion: the modulus margin [8].

The architecture of the Cartesian network of SS-ADPLLs is described in section II. Section III is dedicated to stability and performance analysis of the Cartesian network. It is shown

that the filter coefficients must satisfy a certain condition in order to synchronize mutually the nodes of the network. In section IV, the validity of our theoretical results is illustrated with simulation results. Finally, conclusions are presented in section V.

II. Architecture Description

As an example, the architecture of a 16-nodes Cartesian network of coupled SS-ADPLLs is presented in Fig. 2 in which each circle represents the SS-ADPLL described in Fig.1.

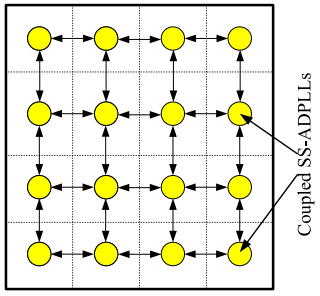

Fig. 2. Architecture of a 16-nodes cartesian network.

It is theoretically demonstrated in [1] that if the phase detectors have linear characteristics for small phase errors and if the filter is a Proportional-Integral (PI) filter, the state at which all phase errors (including the phase error between the external reference and the local clock of the corresponding node) are zeros is a stable state of the system for a certain set of parameters of the filter coefficients and the DCO gain. The topology of the PFD, measuring the time interval between two events (the rising edges of the inputs), is shown in Fig. 3. The Bang-Bang PFD (BB-PFD) detects the sign of the phase error (*SIGN*) as well as the phase error (*MODE*) between the two inputs. A Time to Digital Converter (TDC) is used to convert the *MODE* signal into a non-signed *m*-bits code to obtain a quasi-linear characteristics for small phase errors. The arithmetic block generate a signed two's complement binary code by multiplying the *SIGN* and the TDC output. Let $t_i[n]$ and $t_r[n]$ designate the time at which the n^{th} rising edge of the local and the neighbor clock respectively happen. In the linear framework of the PFD, the timing error (the PFD output) represented by $e_{ri}[n]$ is equal to:

$$e_{ri}[n] = t_r[n] - t_i[n], \tag{1}$$

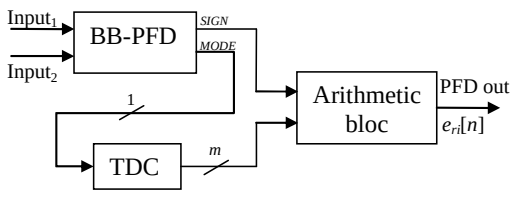

Fig. 3. Topology of the PFD.

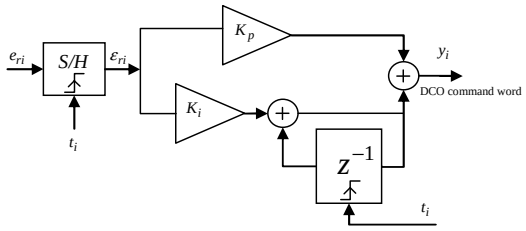

Fig. 4. Topology of the PI filter.

It should be noted that at time $t_i[n]$ (the time at which the filter is sampled) if the local clock is lagging the neighbor clock ($t_r[n] < t_i[n]$), $e_{ri}[n]$ is known by the filter. Contrary if the local clock is leading ($t_r[n] > t_i[n]$), $e_{ri}[n]$ can not be known. Indeed when the local clock is leading, the value known by the filter is the last value generated by the PFD: $e_{ri}[n-1]$. This phenomena is so-called the self-sampling property of the SS-ADPLLs. In order to update the output of the filter ($y_i[n]$) at every rising edge of the local clock, it is then necessary to provide the PI filter with an estimation of $e_{ri}[n]$, whenever the local clock is leading. Considering the topology of the PI filter given in Fig. 4, $y_i[n]$ is governed as follow:

$$y_i[n] = y_i[n-1] + K_1\epsilon_{ri}[n] + K_2\epsilon_{ri}[n-1], \tag{2}$$

where K_1 is equal to $K_p + K_i$, K_2 is equal to $-K_p$ and $\epsilon_{ri}[n]$ is the filter input given by:

$$\epsilon_{ri}[n] = \begin{cases} e_{ri}[n] & \text{if } e_{ri}[n] \leq 0, \\ e_{ri}[n-1] & \text{otherwise.} \end{cases} \tag{3}$$

The presented 16-nodes Cartesian network of the SS-ADPLL is actually in the physical implementation phase in CMOS $65nm$ technology in the context of the HODISS project funded by the ANR AFRU program. The interested reader can refer to [7] for more informations about transistor-level implementation of the blocks since this paper addresses our approach to simplify the stability and the performance analysis. In the next section the construction of the corresponding average system and the application of the modulus margin is discussed.

III. Stability and Performance

As mentioned in section I, networks of SS-ADPLLs can be described as PLSs. In [6] we have explored this method to determine the stability domain of networks of SS-ADPLLs. It is shown that the stability analysis based on Piecewise-Quadratic Lyapunov Functions (PQLFs), which is the most rigorous approach, is particularly difficult to establish and costly in computing time as the network size increases. Moreover, it cannot be applied to all sorts of SS-ADPLLs and yields only sufficient stability conditions. Here we focus on the determination of the optimum coefficients of the digital filter to ensure the best possible stability related performance of Cartesian networks of SS-ADPLLs of arbitrary size. Our approach consists in constructing an corresponding linear average system

of the network. It is then straightforward to find an optimum necessary condition for the stability related performance of the whole network by computing the roots of its characteristic polynomial. In order to quantify this performance one may use the modulus margin which is a linear stability related performance criterion [8]. The modulus margin characterizes the minimum distance between the Nyquist plot of the open-loop system and the critical point $[-1,\ j0]$. An optimal design of the self-sampled network can be obtained by choosing the coefficients K_1 and K_2 which maximize the modulus margin of the average network. Alternatively, a robust design can be obtained by choosing these coefficients so that variations in them will only induce small changes in the modulus margin of the network, and hence in its settling time and performance.

A Cartesian network of SS-ADPLLs consists in a rectangular (two-dimensional) grid of nodes. Each node can be connected to at most 4 neighbors (Fig. 2). Assuming that, for an autonomous network in which there is no external reference, $t_k[n]$ is the n^{th} rising edge of the local clock of the k^{th} node given by:

$$t_k[n+1] = t_k[n] + T_k + g.y_k[n], \tag{4}$$

where T_k is the period of the DCO internal clock, g is a multiplicative coefficients which corresponds to the DCO gain and $y_k[n]$ is the filter output given by (2). Then the input of the filter of the k^{th} node on the n^{th} rising edge of the local clock $t_k[n]$ is equal to:

$$\epsilon_k[n] = \frac{1}{|V_k|}\sum_{l\in V_k}\epsilon_{lk}[n], \tag{5}$$

with:

$$\epsilon_{lk}[n] = \begin{cases} e_{lk}[n] & \text{if } e_{lk}[n] \leq 0 \\ e_{lk}[n-1] & \text{otherwise,} \end{cases} \tag{6}$$

and:

$$e_{lk}[n] = t_l[n] - t_k[n] = -e_{kl}[n]. \tag{7}$$

where V_k is the set of the indices of the nodes in a neighborhood of the k^{th} node and $|V_k|$ is the cardinal of V_k, i.e. $|V_k|$ is equal to 2 for corner nodes, 3 for edge nodes and 4 otherwise. From (6) to (7), the following fundamental equality can be derived:

$$\epsilon_{lk} - \epsilon_{kl} = e_{lk}[n] + e_{lk}[n-1]. \tag{8}$$

Let us also define $\epsilon[n]$ a vector whose k^{th} coordinate is $\epsilon_k[n]$ and $\mathbf{e}[n]$, a vector whose k^{th} coordinate is:

$$e_k[n] = \frac{1}{|V_k|}\sum_{l\in V_k} e_{lk}[n]. \tag{9}$$

Each SS-ADPLL uses $\epsilon_k[n]$ (5) to update the local filter output at time $t_k[n]$, as in [7]. One may then assemble the equations governing the whole network:

$$\mathbf{e}[n+1] - 2\mathbf{e}[n] + \mathbf{e}[n-1] = -\mathbf{L}(K_1\epsilon[n] + K_2\epsilon[n-1]). \tag{10}$$

where $\mathbf{L}$ is the normalized Laplacian matrix of the network, defined as:

$$L_{kl} = \begin{cases} 1 & \text{if } k = l \\ -\frac{1}{|V_k|} & \text{if } l \in V_k \\ 0 & \text{otherwise.} \end{cases} \tag{11}$$

Definition 1 (The average system)**.** An average system is defined by replacing $\epsilon[n]$ in (10) by:

$$\tilde{\epsilon}[n] = \frac{1}{2}(\mathbf{e}[n] + \mathbf{e}[n-1]). \tag{12}$$

The resulting system is linear and its stability can be deduced from the position of its poles. The stability domain of a 4-nodes network obtained by transient simulation of the real non-linear network and those of the average system are shown respectively in Fig. 5 and Fig. 6. The studies in [7] and the comparison between Fig. 5 and Fig. 6 permit to show that the networks behaves as the average system corresponding for the class of ADPLLs considered in this study. This observation reinforces the approach used and allows to meet the constraints that ensure the best stability related performance possible for the system.

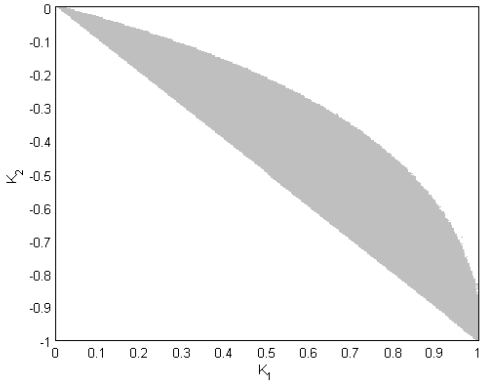

Fig. 5. Stability domain (gray area) of the nonlinear SS-ADPLLs 4-nodes network determined by transient simulation.

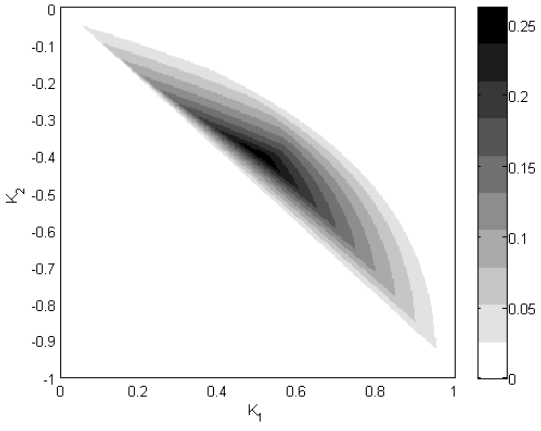

Fig. 6. Stability domain (gray and black area) of the average system corresponding to the 4-nodes network in function of the modulus margin.

IV. Validity and results

The stability domains derived from the characteristic polynomials of (10) are represented in Fig. 6 and Fig. 7 for different sizes of the Cartesian network. The simulations are

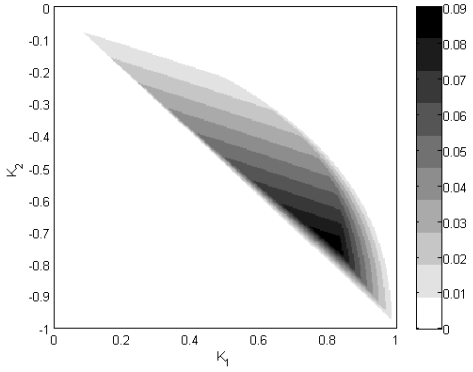

Fig. 7. Stability domain (gray and black area) of the average system corresponding to the 16-nodes network in function of the modulus margin.

done for normalized parameters. As it is shown, the optimum values of K_1 and K_2 coefficients are decreased from small to large size of the network. It means that the open loop gain of each SS-ADPLL must be diminished regarding the relation between K_1, K_2 and K_p, K_i given in section II. The sum of the PFDs outputs ($e_i[n]$) for each node of the 4-nodes network is shown in Fig. 8 for the optimum coefficients found from Fig. 6 ($K_1 = 0.51$ and $K_2 = -0.4$). As it is shown, all

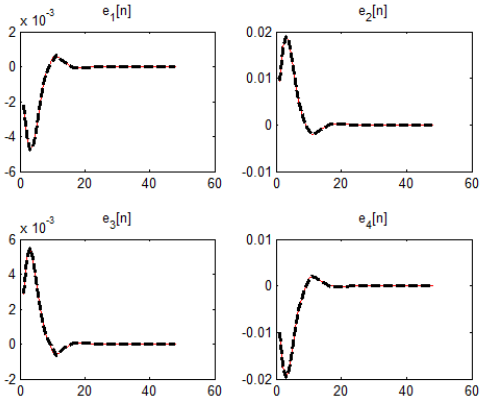

Fig. 8. The sum of the PFDs outputs ($e_i[n]$) for each node of the 4-nodes network for the optimum coefficients ($K_1 = 0.51$ and $K_2 = -0.4$).

the $e_i[n]$ converge to zero after a short settling time which means a global synchronization of the network. Moreover, for a 16-nodes network, the sum of the PFDs output of an arbitrary node is compared for the optimum and the non-optimum parameters in Fig. 9. The comparison between the settling time and the oscillation amplitude between the two cases proves the necessity to find the optimum parameters. These observations lead us to the conclusion that the average system is a good basis for the design of Cartesian networks of SS-ADPLLs.

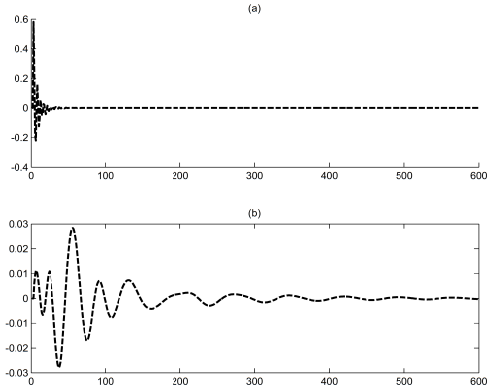

Fig. 9. Comparison between the sum of the PFDs outputs for an arbitrary node of the 16-nodes network for the optimum (a) and the non-optimum (b) coefficients.

V. Conclusions

The main contribution of this paper was consisted in determining appropriate specifications for the filter coefficients in order to guarantee a robust stability of Cartesian networks of SS-ADPLLs. Our study indicates that a stability taking into account the performance criteria of an autonomous cartesian network can be established through the stability analysis of an corresponding linear average system. Transient simulations have shown the reliability of this approach although rigorous demonstration remains to be established. The influence of an external reference and the non-linear properties of the PFD on the stability performance are the subjects of the works that will follow.

Acknowledgment

This work was supported by the French National Agency of Research (ANR) through the HODISS project.

References

[1] G.A. Pratt and J. Nguyen, *Distributed Synchronous Clocking*, IEEE Trans. on Parallel and Distributed System, vol. 6, pp. 314-328, 1995.

[2] V. Gutnik and A.P. Chandrakasan, *Active GHz Clock Network Using Distributed PLLs*, IEEE Journal of Solid State Circuits, vol. 35, pp. 1553-1560, 2000.

[3] E.G. Friedman, *Design and Analysis of a Hierarchical Clock Distribution System for Synchronous Standard Cell/Macrocell VLSI*, IEEE Journal of Solid State Circuits, vol. 21, pp. 240-246, 1986.

[4] M. Saint-Laurent and M. Swaminathan, *A Multi-PLL Clock Distribution Architecture for Gigascale Integration*, IEEE Computer Society Workshop on VLSI, pp. 30-35, 2001.

[5] Y. Xiaoji, L. Peng, Z. Min and R. Panda, *Scalable Analysis of Mesh-Based Clock Distribution Networks Using Application-Specific Reduced Order Modeling*, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 29, pp. 1342-1353, 2010.

[6] J.M. Akre, J. Juillard, S. Olaru and D. Galayko, *Determination of the Behavior of Self-Sampled Digital Phase-Locked Loops*, 53rd IEEE Int. MWSCAS'10, pp. 1089-1092, Seattle, Washington(USA), August 2010.

[7] M. Javidan, E. Zianbetov, D. Galayko, E. Colinet and J. Juillard, *All-digital PLL array provides reliable distributed clock for SOCs*, IEEE International Symposium on Circuits and Systems (ISCAS), Riodejaneiro, Brazil, May 2011.

[8] C.S. Banyasz and L. Keviczky, *A New Gap Metric for Robustness Measure and Regulator Design*, 17th IEEE Mediterranean Conference on Control and Automation (MED '09), Thessaloniki, Greece, June 2009.